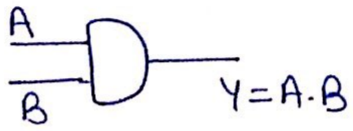
ELECTRONICS

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→ Boolean Algebra:

1) NOT theorem: 

2) AND theorem: 

3) OR theorem: 

4) Distributive theorem: $Y = (A+B)(A+C) = A+BC$

$$Y = A+\bar{B}C = (A+\bar{B})(A+C)$$

example: minimize the following expression

① $Z = x+\bar{x}y$

Soln. $Z = (x+\bar{x})(x+y)$

$= 1.(x+y) \Rightarrow \boxed{x+y}$

② $y = (\bar{A}+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+B+\bar{C})$

Soln. let $\bar{A}+\bar{B} = x$

$y = (x+\bar{C})(x+C)(\bar{A}+B+\bar{C})$

$y = (x.x + C\bar{C})(\bar{A}+B+\bar{C})$

$y = x(\bar{A}+B+\bar{C}) \Rightarrow (\bar{A}+\bar{B})(\bar{A}+B+\bar{C})$

$y = \bar{A} + B\bar{B} + \bar{B}\bar{C}$

$\boxed{y = \bar{A}+\bar{B}\bar{C}}$

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→ **SOP & POS Form:**

Sum of Products (SOP)	Product of Sum (POS)
→ used when o/p of any digital CKT is HIGH	→ used when o/p of any digital CKT is Low
→ minterm : '1'	→ maxterm : '0'
→ e.g. 5 : 101 $A\bar{B}C = 1$	→ e.g 5 : 101 $(\bar{A}+B+\bar{C}) = 0$
→ $F(A,B) = \Sigma m(0,2)$	→ $F(A,B) = \Pi M(1,3)$

Canonical Form: either SOP or POS expression without reducing number of variables.

example: For the given function:

$$F(A,B,C) = A+\bar{B}C$$

① write in terms of canonical SOP form
② Identify the no. of minterms present
③ Identify no. of maxterms
④ write in terms of canonical POS.

Sol^{no}- ① $Y_{SOP} = A+\bar{B}C = 1$

when $A=1$, $\bar{B}C = 01$

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

canonical SOP:

$$\bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

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② minterms = no. of canonical SOP terms

= ⑤

③ maxterms = total terms - minterms

$= (2)^3 - 5 \Rightarrow ③$

④ canonical POS = $\Pi M(0, 2, 3)$

$= \boxed{(A+B+C)(A+\bar{B}+C)(A+\bar{B}+\bar{C})}$

Note: $\boxed{Y_{POS} = Y_{SOP}}$ (always)

Que 2 For the given expression:

$F(A, B, C, D, E) = A + \bar{D}E$

Find no. of maxterms & minterms?

a) 12, 20 b) 20, 12 c) 16, 16 d) 14, 18

Sol$^{n}_{o}$- $Y = A + \bar{D}E = 1$

when $A = 1 \Rightarrow Y = 1$ (always) → 16 terms

$\bar{D}E = 0, 1 \Rightarrow Y = 1$ → 8 terms

but 4 already counted in $A = 1$

total maxterms = total terms - minterms

minterms = 16 + 4 = ⑳

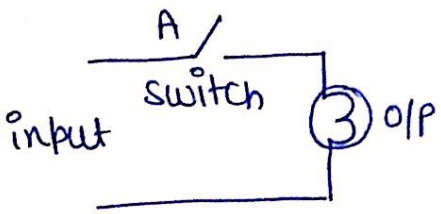
max terms = $(2)^5 - 20 = ⑫$

A

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→ Basic gates using switching circuit:

1) Switch in Series with output:

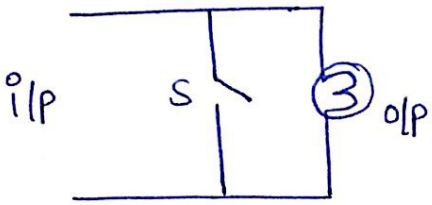


Close: 1 ; Open : 0

input	output
0	0
1	1

→ act as a Buffer (voltage follower, commom collector configuration)

2) Switch in Parallel with output:

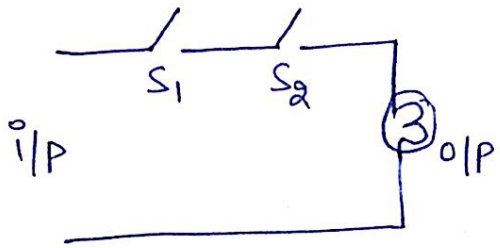


input	output
0	1
1	0
A	$\overline{A}$

→ NOT gate (Invertor)

→ NOT gate always delay.

3) two switch in series with output:

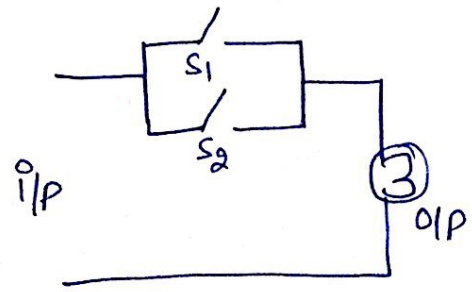


S_1	S_2	o/p
0	0	0
0	1	0
1	0	0
1	1	1

→ AND gate

o/p = A.B

4) two switchs in Parallel:



S_1	S_2	o/p
0	0	0
0	1	1
1	0	1
1	1	1

→ OR gate

o/p = A+B

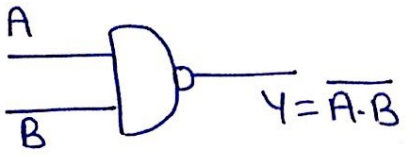
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→ **Universal gates:** (Uncontrolled gates)

any digital ckt can be implemented by using these gates.

1) **NAND gate:**

AND + NOT → NAND



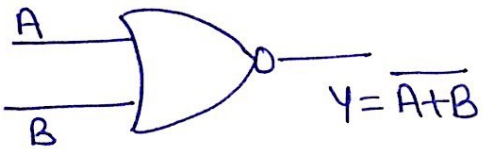
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

→ Truth Table

*** → If any i/p = 0 then o/p = 1

2) **NOR gate:**

OR + NOT → NOR



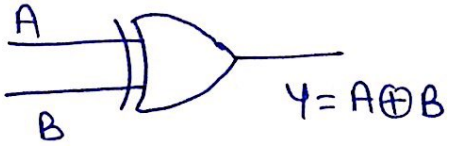
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

→ Truth table

*** → If any i/p = 1 then o/p = 0

→ **Airthmatic gates:**

1) **Exclusive-OR gate:** (Controlled gate)



$Y = \overline{A}B + A\overline{B}$

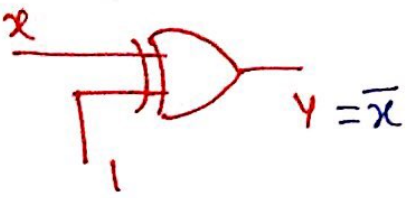
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

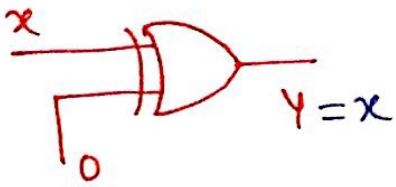
*** → ① If all i/p same ⇒ o/p = 0

If all i/p different ⇒ o/p = 1

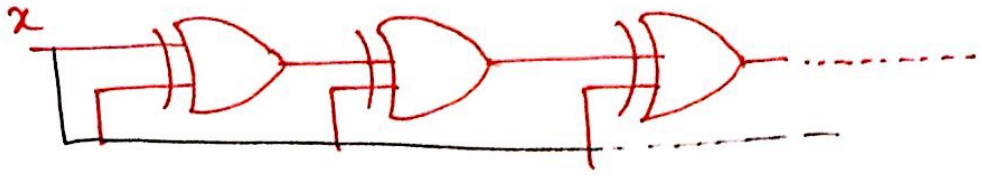
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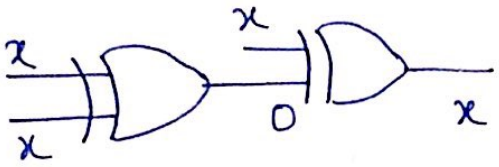
② 

③ 

Que 1 Determine the output after 100 Ex-OR gates of the following circuit:



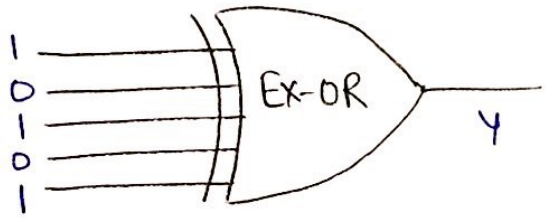
a) 0 b) x c) $\bar{x}$ d) 1

Soln:- 

O/P after odd no. of Ex-OR = 0 **B**

O/P after even no. of Ex-OR gates = x

Note: Ex-OR is a odd function of one(1).



3 times 1
i.e odd fxn
⇒ **Y = 1**

Que 2 For the given logical expression shown:

$$y = \underline{A \oplus B} \oplus \underline{A \oplus B} \oplus \underline{A \oplus B} \oplus \underline{A \oplus B}$$

determined minimized expression.

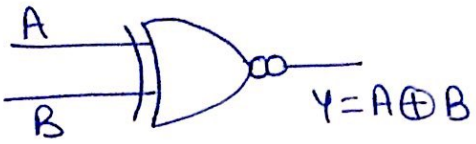
Soln:- let $A \oplus B = x$

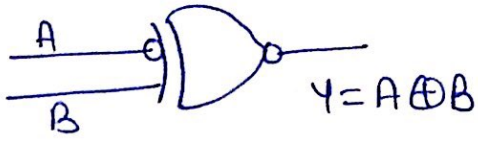
$$y = \underline{x \oplus x} \oplus \underline{x \oplus x} = 0 \oplus 0 = \boxed{0}$$

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Note: Ex-OR & Ex-NOR gates are used to control the operation of Bulb in the staircase applications.

*** → Put any two bubble in Ex-OR gate, output will be same i.e





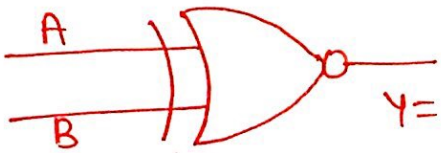
*** → For n number of variable (Ex-OR gate)

no. of minterms : $2^n/2 = 2^{n-1}$

no. of maxterms : $2^n/2 = 2^{n-1}$

2) Ex-NOR gate: (equality detector)

Ex-OR + NOT ⟶ Ex-NOR

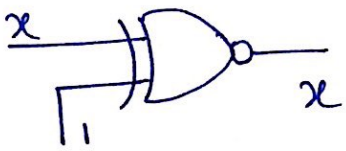


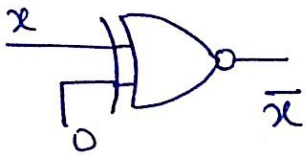
$Y = \overline{A \oplus B} = A \odot B = AB + \bar{A}\bar{B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

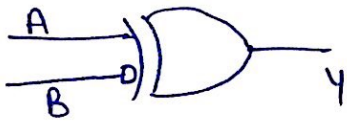
*** → ① if both input : same then output : one (1)

*** → coincidence logic gate.

② 

③ 

→ Place a single bubble anywhere in EXNOR CKT output will be same i.e A⊙B

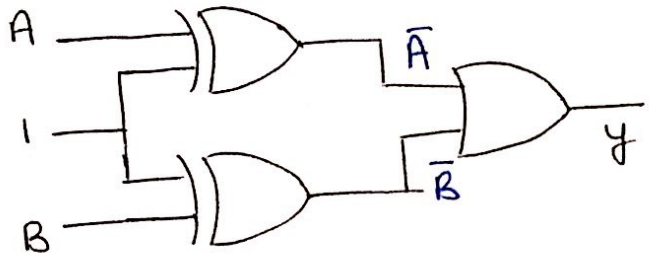


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→ **Demorgan's Theorem:**

① $\overline{A+B} = \overline{A} \cdot \overline{B}$ ② $\overline{A \cdot B} = \overline{A} + \overline{B}$

Que 3 Determine output y for the given circuit:

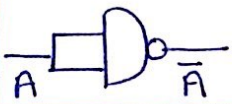
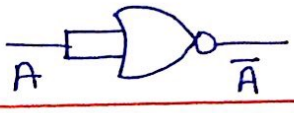
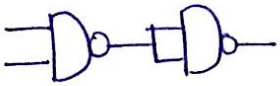
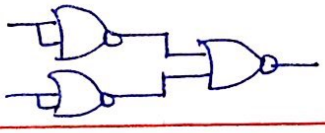
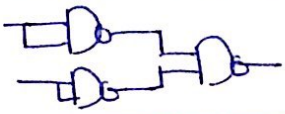
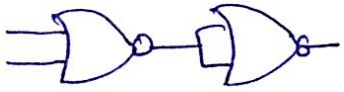
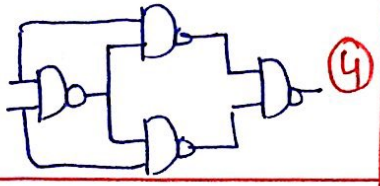
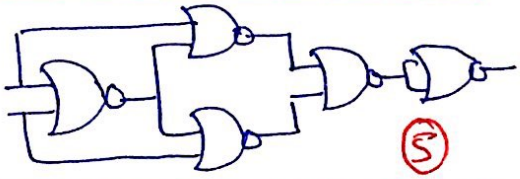


a) $\overline{A+B}$ b) $\overline{A \cdot B}$

c) $\overline{A} \cdot \overline{B}$ d) $\overline{A} \cdot B$

Sol^n:- $y = \overline{A} + \overline{B} = \overline{A \cdot B}$ **B**

→ **minimum number of NAND / NOR gates:**

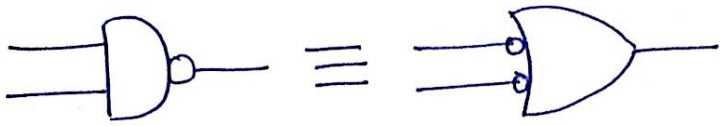
Gates	no. of Nand gates	no. of NOR gates
NOT	 ①	 ①
AND	 ②	 ③
OR	 ③	 ②
NAND	AND+NOT, NAND ①	OR+NOT ④
NOR	AND+NOT ④	NOR ①
EX-OR	 ④	 ⑤
EX-NOR	EX-OR +NOT ⑤	EX-OR -NOT ④

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→ Implementation of SOP form logical expression by using minimum number of NAND gates:

1) implement the logical expression by using basic gates.

2) Place a bubble at the O/P of AND gate and at the input of OR gate.



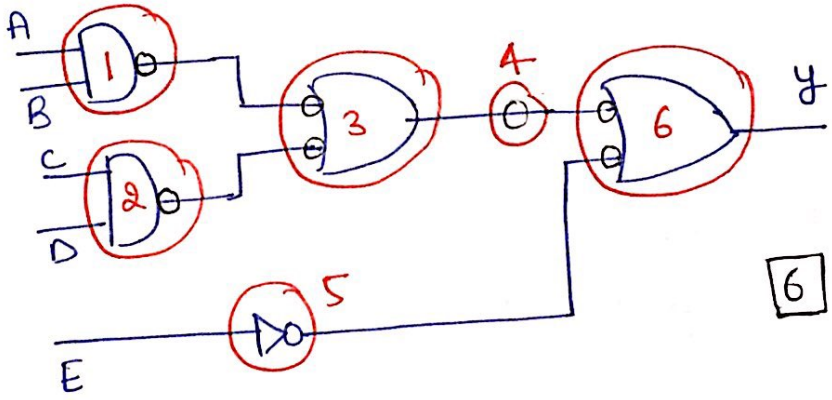
So, that the effect of bubble gets cancel out

3) count the number of gates.

example:

① $y = AB + CD + \bar{E}$

Soln:-

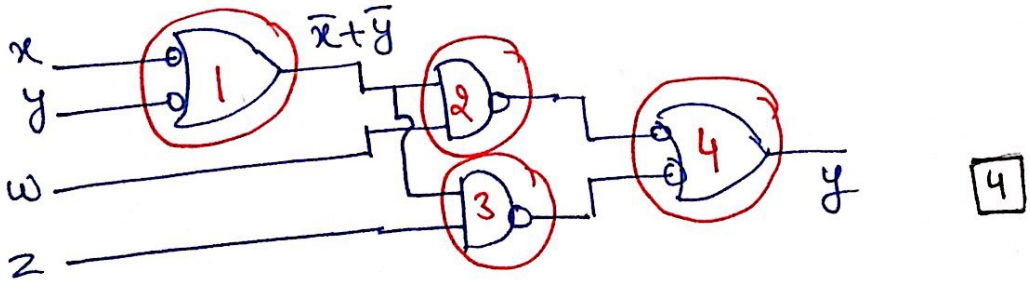


6

② $y = (\bar{x}+\bar{y})(w+z)$

$y = \bar{x}(w+z) + \bar{y}(w+z)$

$= w(\bar{x}+\bar{y}) + z(\bar{x}+\bar{y})$



4

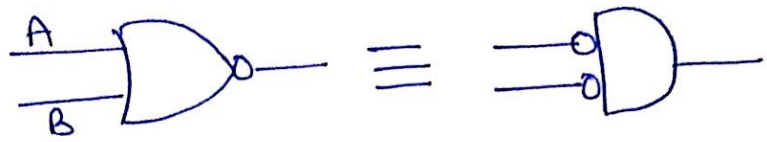
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→ **Implementation of POS form expression by using minimum number of two i/p NOR gates:**

1) implement the logical expression by using basic gates.

2) Place a bubble at the output of OR gate and at the input of AND gate.

Eg.

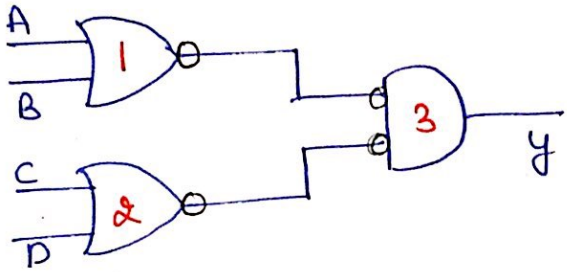


3) count the number of gates.

example:

① $y = (A+B)(C+D)$

Soln:-

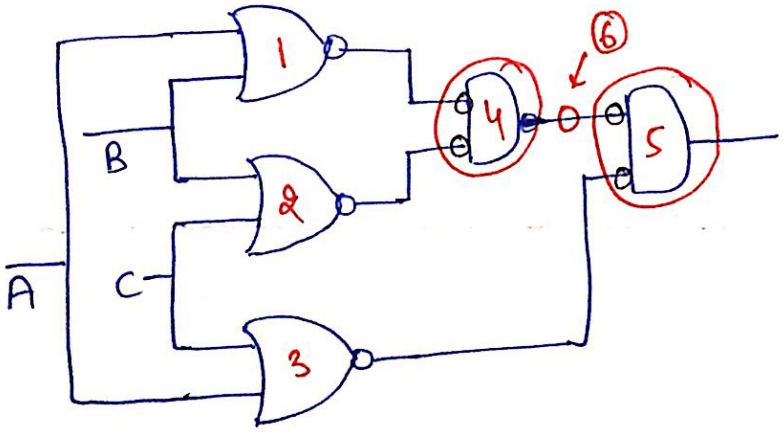


3

② $y = AB + BC + AC$

→ By NAND = 6 NAND gates

→ By NOR = 6 NOR gates

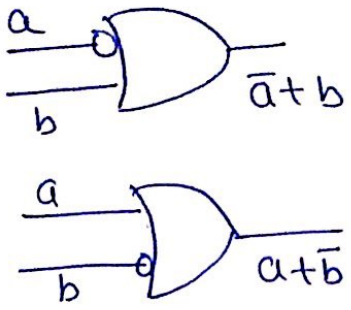


6

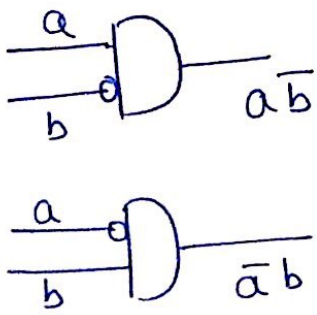
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→ **Inhibitor:**

① $\bar{a}+b$ OR $a+\bar{b}$



② $a\bar{b}$ OR $\bar{a}b$



***→

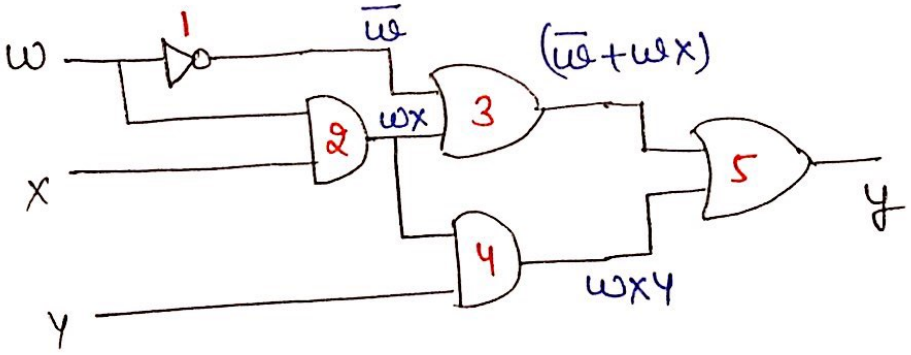
① $a \oplus b \neq a \odot b$

$a \oplus b \oplus c \oplus d \neq a \odot b \odot c \odot d$ } when even

② $a \oplus b \oplus c = a \odot b \odot c$

$a \oplus b \oplus c \oplus d \oplus e = a \odot b \odot c \odot d \odot e$ } when odd

Example: For the given circuit diagram identify the logic circuit which is Redudent (waste)



soln: $Y = (\bar{w}+wx) + wxy$

$= \bar{w} + wx(1+y)$

$= \bar{w} + wx$

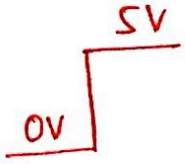
gate ④ is not required.

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→ **Negative logic and Positive logic:**

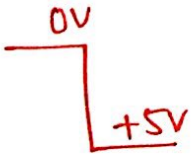
Positive logic: whenever higher values are assigned to higher potential and lower values are assigned to lower potential.

e.g. logic '1' = 5V
logic '0' = 0V



Negative logic: whenever higher values are assigned to lower potential and lower values are assigned to higher potential.

e.g. logic '1' = 0 V
logic '0' = +5V



→ **Duality:**

Process of conversion from +ve logic to -ve logic & vice-versa called Duality.

Steps:

1> 0 ⟷ 1

2> · ⟷ +

3> variables must be same.

example: Positive logic OR gate is equivalent to:

a> -ve logic OR gate

~~b>~~ -ve logic AND gate

c> -ve logic NAND gate

d> -ve logic NOR gate

Soln:-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(+ve logic) ↑ OR

→ -ve logic

A	B
1	1
1	0
0	1
0	0

(AND)

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① $A.B$ (AND) $\xleftrightarrow{D}$ $A+B$ (OR)

② $\overline{A.B}$ (NAND) $\xleftrightarrow{D}$ $\overline{A+B}$ (NOR)

③ $\overline{A}B+A\overline{B}$ (EXOR) $\xleftrightarrow{D}$ $AB+\overline{A}\overline{B}$ (EXNOR)

↑ +ve logic ↑ −ve logic

example:

① Find the dual of given expression:

$$f = AB+CD$$

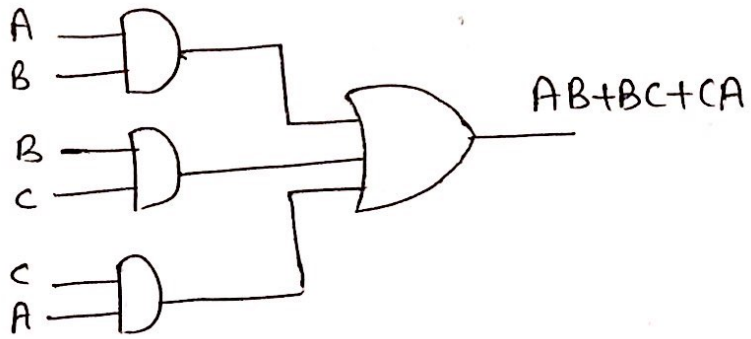
Soln:- $f_D = (A+B).(C+D)$ $\quad \cdot \longrightarrow +$, $+ \longrightarrow \cdot$

Note: If single time dual results in some expression, such expression are called **self Dual**

e.g. ① $f = (A+B)(B+C)(A+C)$

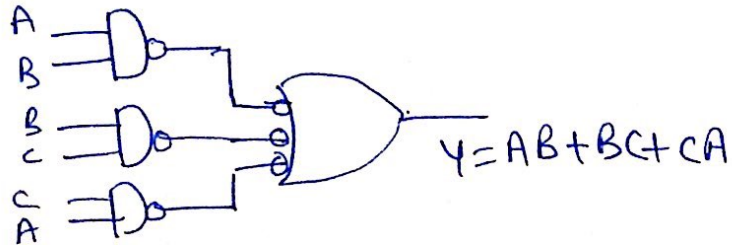
② $f = \overline{A}\overline{B}+\overline{B}\overline{C}+\overline{A}\overline{C}$

② If all the gates are replaced by NAND gates then the resultant:



a) f b) f_D c) f^1 d) $\overline{f_d}$

Soln:-



A

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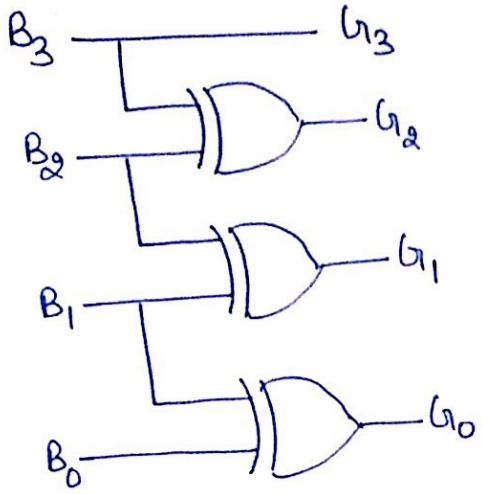
→ K-Map:

outer structure: Based on Gray Code

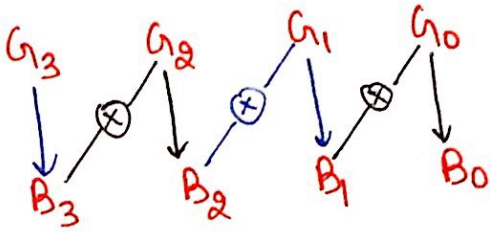
graphical Representation of Boolean expression.

- → unweighted code
- → cyclic
- → unit distance code

Binary to Gray conversion:



Gray to Binary conversion:

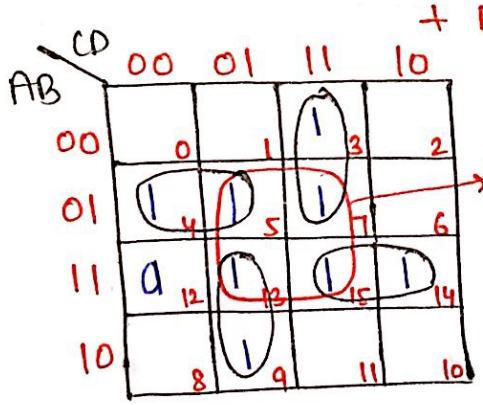


example:

① minimize the given expression:

$$Y = \bar{A}BCD + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + ABC\bar{D} + ABCD$$

Soln:-



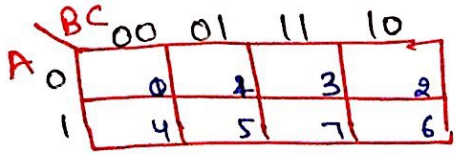
$\bar{A}CD = \underbrace{\bar{A}BCD}_{7} + \underbrace{\bar{A}\bar{B}CD}_{3}$

$\bar{A}B\bar{C} = \underbrace{\bar{A}B\bar{C}D}_{5} + \underbrace{\bar{A}B\bar{C}\bar{D}}_{4}$

$A\bar{C}D = \underbrace{A\bar{B}\bar{C}D}_{9} + \underbrace{AB\bar{C}D}_{13}$; $ABC = \underbrace{ABCD}_{15} + \underbrace{ABC\bar{D}}_{14}$

$$\boxed{Y = \bar{A}B\bar{C} + \bar{A}CD + A\bar{C}D + ABC}$$

Note: For 3 variable



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→ Number System:

Base: it represents the number of digits used in any number system.

Number System	Base	no. of digits
Binary	2	0, 1
Septal	7	0, 1, 2, 3, 4, 5, 6
Octal	8	0, 1, 2, 3, 4, 5, 6, 7
Decimal	10	0–9
Hexadecimal	16	0–9, A, B, C, D, E, F

1) Decimal to other conversion:

a) $(25.625)_{10} = (____)_2$

2 | 25		
2 | 12	1	↑ LSB
2 | 6	0	
2 | 3	0	
2 | 1	1	
		MSB

$0.625 \times 2 = (1).25$
$0.25 \times 2 = (0).5$
$0.5 \times 2 = (1).0$ ↓

$(11001.101)_2$ Ans.

b) Determine r_1 and r_2:

$(235)_{r_1} = (565)_{10} = (1065)_{r_2}$

a) 8, 11 b) 8, 16
c) 12, (8) d) 16, (8)

565 < 1065
↓ Base 10 ↓ Base < 10

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16	565	
16	35	5 ↑
	2	3

D

$(235)_{16} \Rightarrow r_1 = 16 \;\&\; r_2 = 8$

③ Determine the value of x for the given representation: $(123)_x = (12x)_3$

a) 3 b) −4 c) 5 d) none

Soln. $(123)_x = (12x)_3$

$3 = x$ not Possible

$5 = x$ ——

$-4 = x$ ——

D

Note: Base of no. system $\propto \frac{1}{\text{no. inside argument.}}$

② Others to Decimal conversion:

$(110110.101)_2 = (\text{———})_{10}$

$1\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 0\times2^0$

$= 32 + 16 + 0 + 4 + 2 + 0$

$= 54$

$.101 = 1\times\frac{1}{2} + 0\times\frac{1}{2^2} + 1\times\frac{1}{2^3} = .625$

$= (54.625)_{10}$

Note: Octal number ≡ 3-bit binary number

Hexadecimal number ≡ 4-bit binary number

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→ **Complement of Number System:**

1) **(r-1)'s complement:** select the maximum digit of that number system, write it on each and every bit. Perform the subtraction, the resultant will be (r-1)'s complement.

e.g. Find 1's complement of $(1010)_2$?

Soln:-

```
  1 1 1 1
- 1 0 1 0
---------
  0 1 0 1   → (r-1)'s OR 1's complement
```

Here r = 2 for Binary system.

2) **r's complement:** add 1 at LSB of (r-1)'s complement.

e.g. Find r's complement of $(2349)_{10}$?

Soln:-

```
  9 9 9 9
- 2 3 4 9
---------
  7 6 5 0   ← 9's
```

```
  7 6 5 0
+       1
---------
  7 6 5 1   → 10's complement
```

→ **Signed magnitude:**

In the n-bit binary representation MSB will give sign, Rest (n-1) bit will give the magnitude.

e.g.

```
MSB
 1 0 0 1
 ↑ ↑ ↑ ↑
Sign  magnitude
```

MSB → 1 (-ve)
MSB → 0 (+ve)

⇒ (-1)

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→ **Half Adder:**

it Represents two 1-bit addition.



$0+0=0$

$0+1=1$

$1+0=1$

$1+1=10$ (1 ↑ Carry, 0 ↑ Sum)

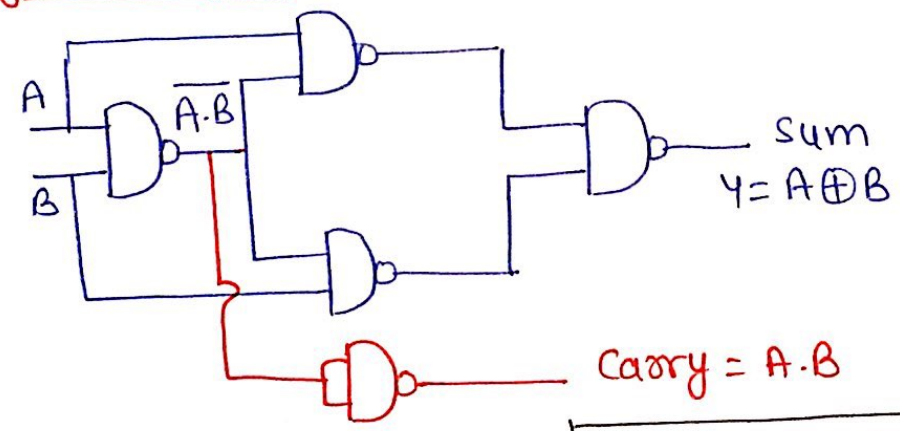
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum = A⊕B, Carry = A.B

*** a Half adder has two inputs & 2 outputs.

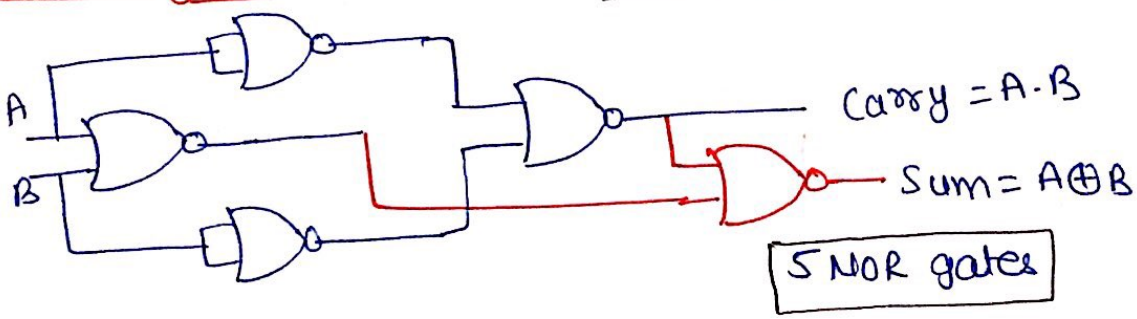
Implementation of Half adder by using minimum number of two i/p NAND/NOR gates:

1) **By NAND gate:**



5 NAND gates

2) **By NOR gate:**

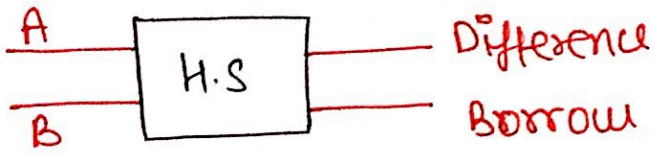


5 NOR gates

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→ **Half Subtractor:**

it represents two 1-bit subtraction.



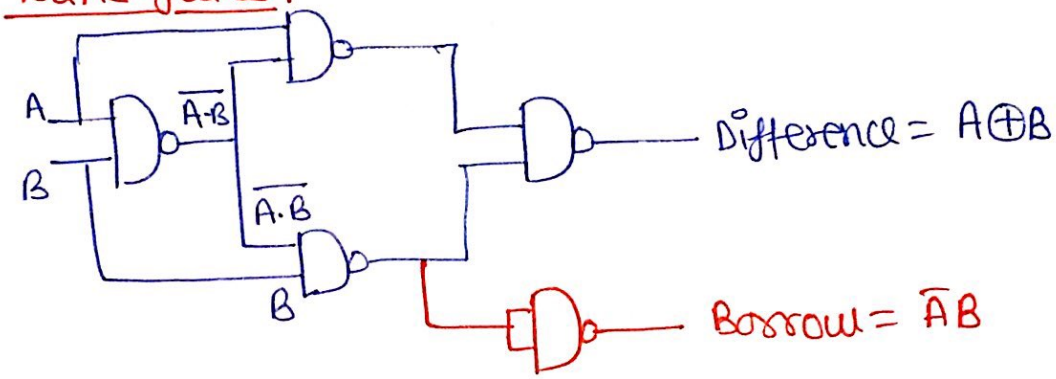
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

↑ $A \oplus B$ ↑ $\bar{A}B$

*** → it has two inputs and two outputs.

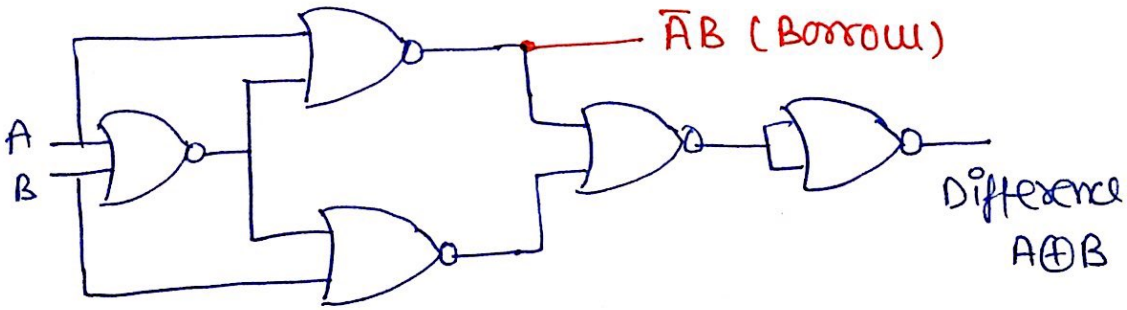
Implementation of Half Subtractor:

1) **By Nand gates:**



5 NAND gates

2) **By NOR gate:**



5 NOR gates

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Note: For Ex-OR gate:

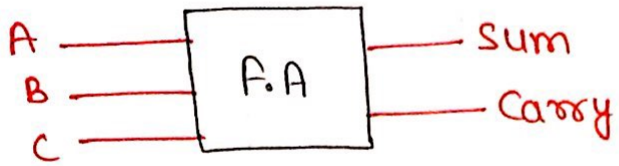
① no. of minterms/maxterms = 2^{n-1}

② self dual for n-variables = $2^{2^{n-1}}$

③ Truth table for n-vabiables = 2^{2^n}

→ **Full Adder:**

It represents 3 bit addition



→ 3 inputs

→ 2 outputs

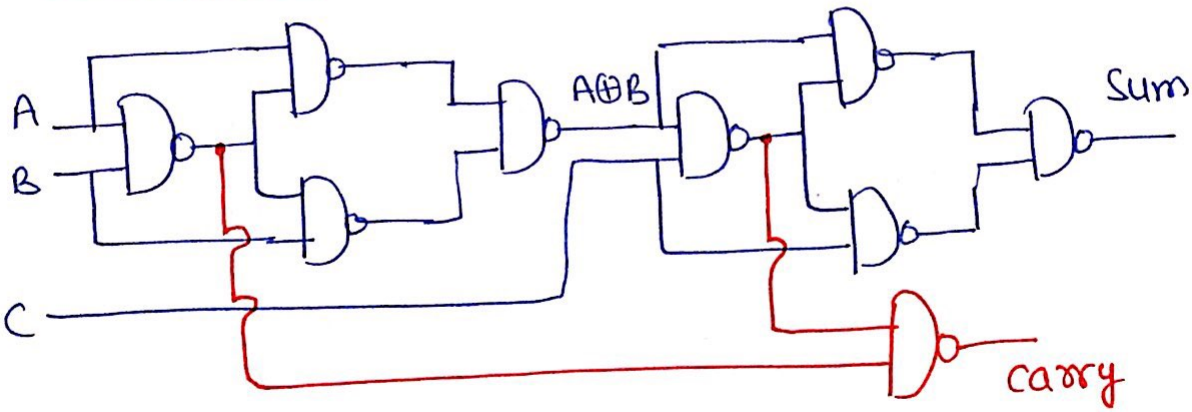
A	B	C	Sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = A \oplus B \oplus C$

$Carry = AB + BC + AC$

implementation of Full Adder by using:

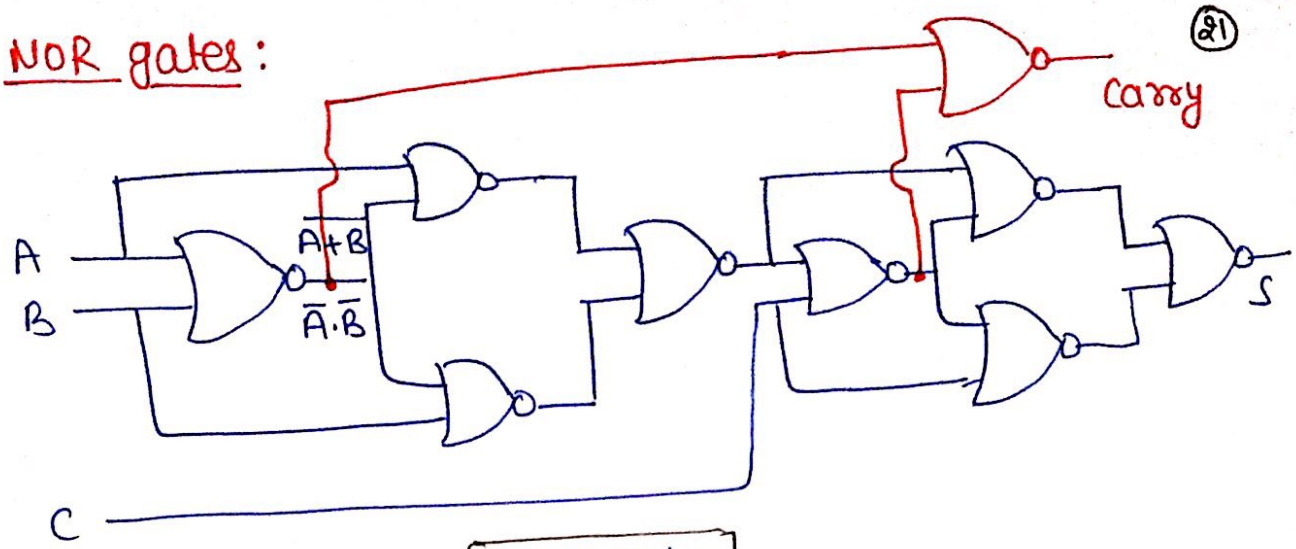
1) NAND gates:



9 NAND gates

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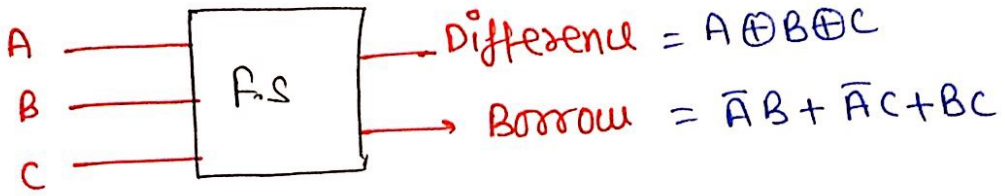
2) NOR gates:



9 NOR gates

→ Full Subtractor:

It represents 3 bit subtraction

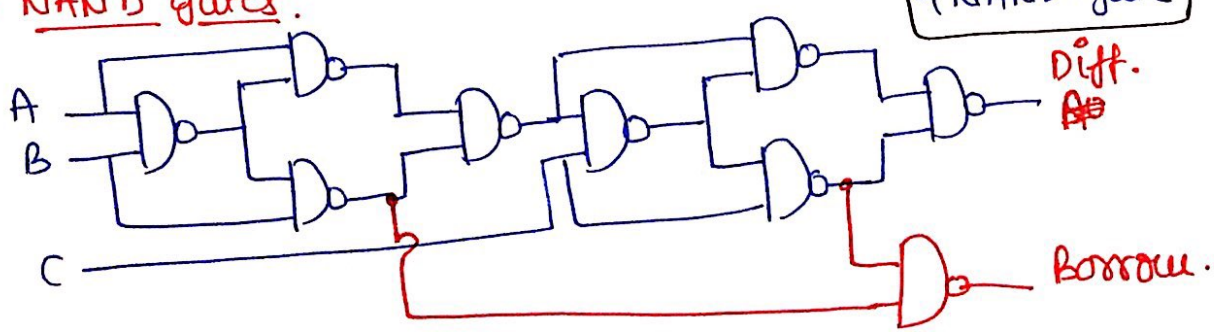


A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

implementation of full subtractor by using:

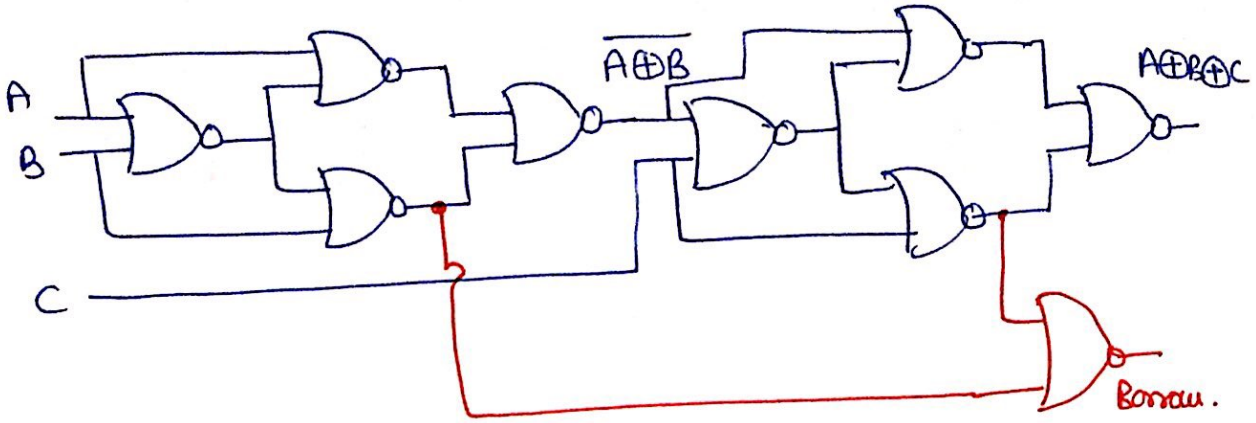
1) NAND gates:

9 NAND gate



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2) By NOR gates:



9 NOR gates

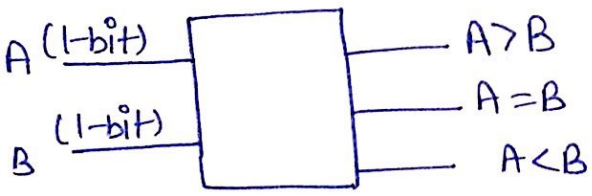
*** → minimum no. of NAND/NOR gates required to implement:

① Half Adder/subtractor: 5 NAND/NOR

② Full Adder/subtractor: 9 NAND/NOR

→ COMPARTOR:

1) Single bit comparator:



→ 2 inputs
→ 3 outputs.

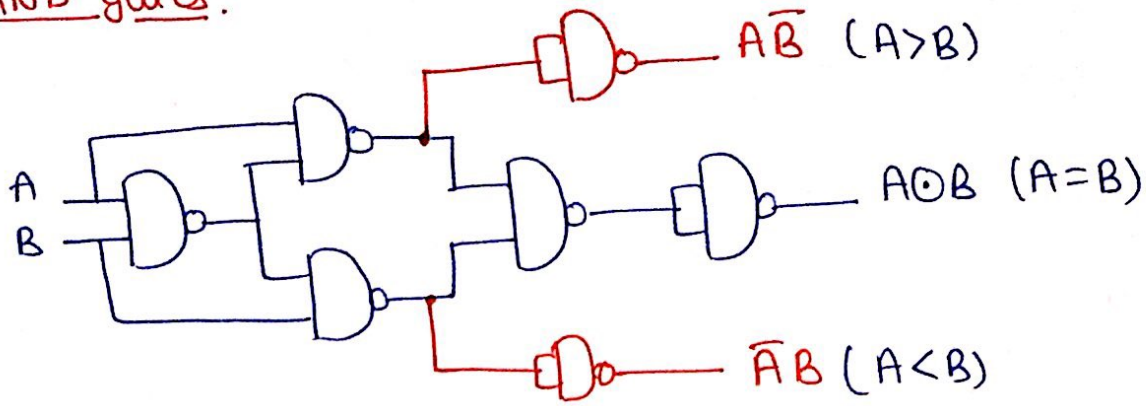
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$A\bar{B}$ $A \odot B$ $\bar{A}B$

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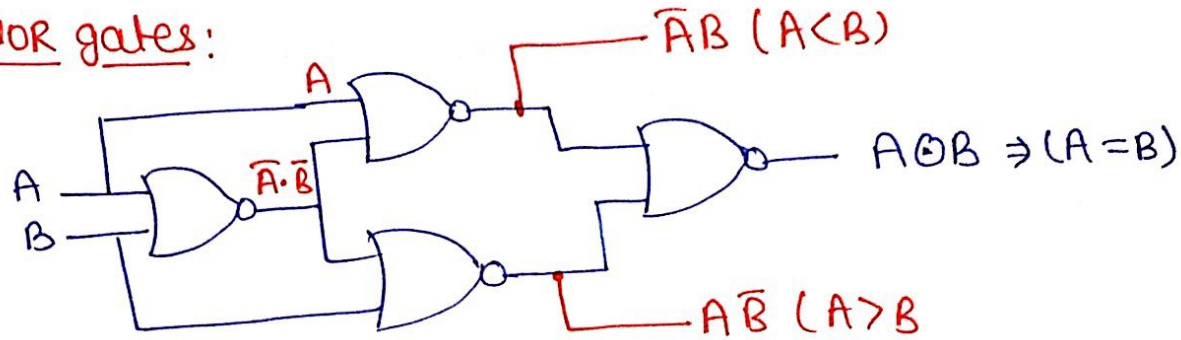
Implementation of single bit comparator by using:

1) NAND gates:



7 NAND gate

2) NOR gates:



4 NOR gates

2) 2-bit comparator:

$A = A_1 A_2$ & $B = B_1 B_2$

For A=B: $A_2 = B_2$ and $A_1 = B_1$

$$y = (A_2 \odot B_2) \cdot (A_1 \odot B_1)$$

For A>B: $A_2 > B_2$ OR $A_2 = B_2$ and $A_1 > B_1$

$$y = A_2 \bar{B_2} + (A_2 \odot B_2) \cdot (A_1 \bar{B_1})$$

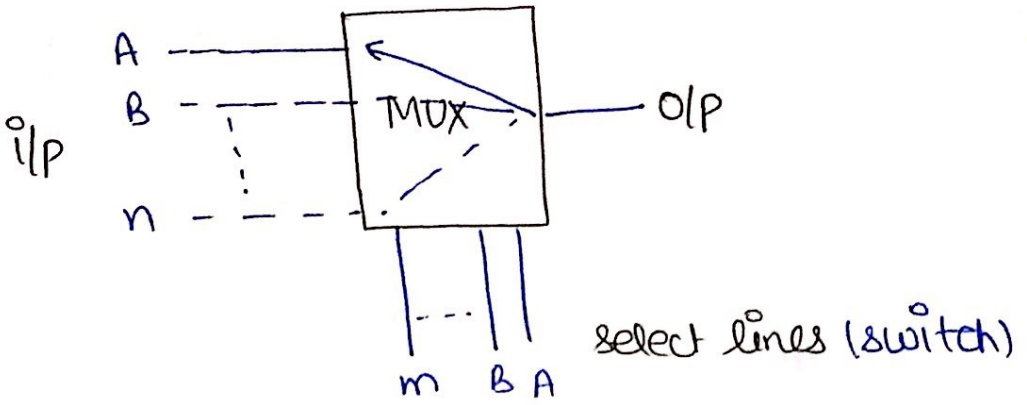
For A<B:

$$y = \bar{A_2} B_2 + (A_2 \odot B_2) \cdot (\bar{A_1} B_1)$$

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→ **Multiplexer (MUX):**

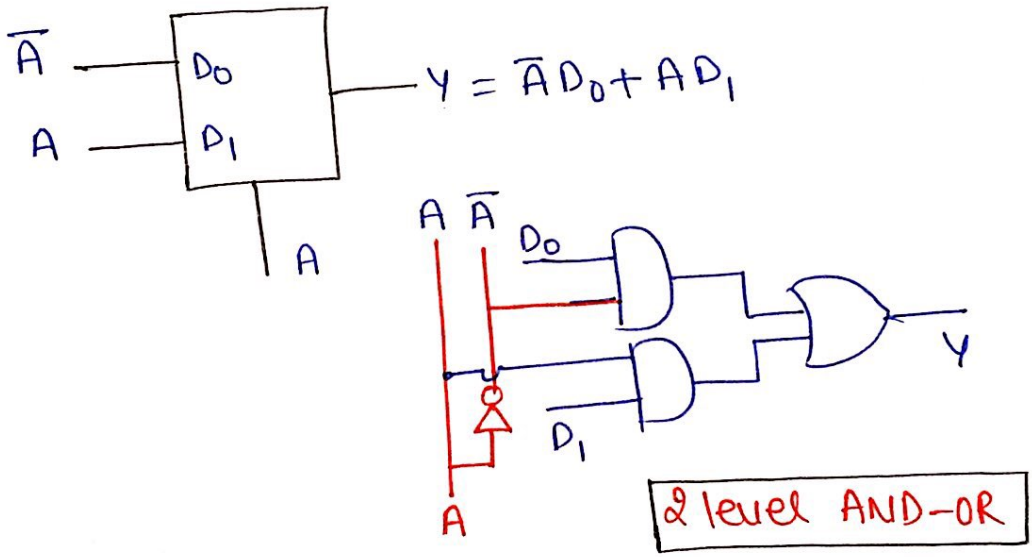
a MUX is Represented by many input & single output line.



internal structure of MUX is represented by a switch.

1) **2x1 MUX:**

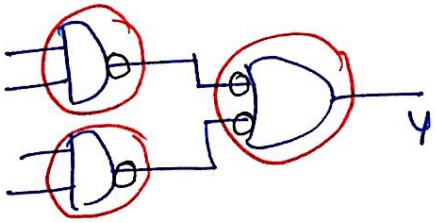
$2^n = 2 \Rightarrow \boxed{n=1}$ → no. of select lines.



Que: For a two level AND-OR circuit can be equally represented by:

a) AND-AND b) OR-AND c) NOR-NOR d) NAND-NAND

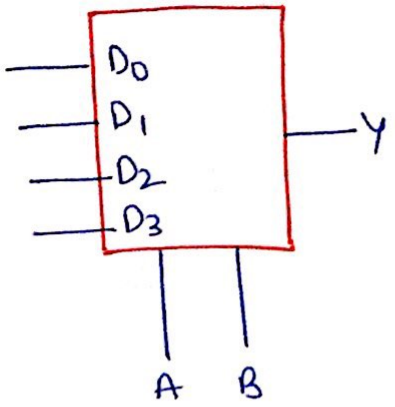
Soln:-



NAND-NAND

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2) 4x1 MUX:



$$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$$

3) 8x1 MUX:

$2^n = 8$

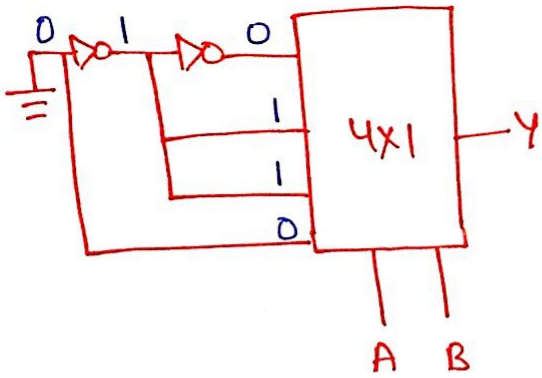
$\Rightarrow \boxed{n=3}$ → select line.

$$Y = \bar{A}\bar{B}\bar{C}D_0 + \bar{A}\bar{B}CD_1 + \bar{A}B\bar{C}D_2 + \bar{A}BCD_3 + A\bar{B}\bar{C}D_4 + A\bar{B}CD_5 + AB\bar{C}D_6 + ABCD_7$$

*** → MUX is a universal circuit.

minimization of logical expression by using MUX:

① minimize:

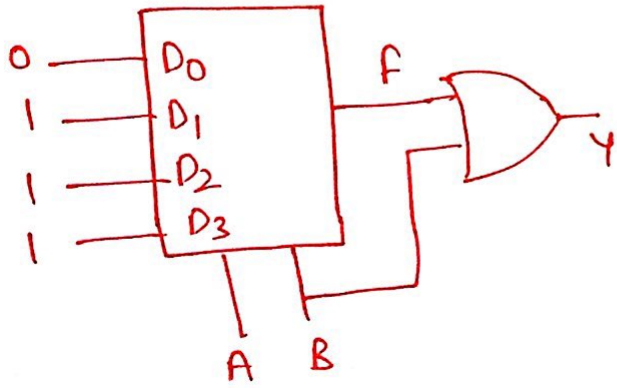


$$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$$

$$Y = \bar{A}B + A\bar{B}$$

$$\boxed{Y = A \oplus B}$$

② minimize:



$$Y = F + B$$

$$= \bar{A}B + A\bar{B} + AB + B$$

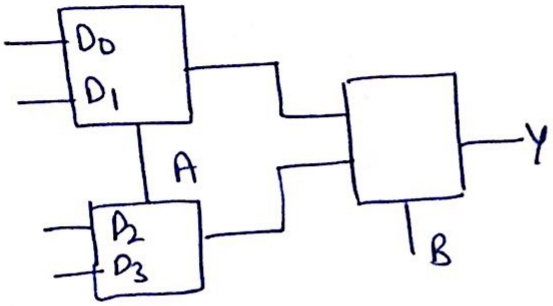
$$= B(\bar{A} + A + 1) + A\bar{B}$$

$$= B + \bar{B}A \Rightarrow \boxed{A + B}$$

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Implementation of Higher order mux by using 2x1 MUX:

① 4x1 MUX by 2x1 MUX.



3 MUX

alternate:

2	4
2	2
	1

2+1 = (3)

2x1 MUX

② 16x1 MUX by 2x1 MUX

2	16
2	8
2	4
2	2
	1

⇒ 8+4+2+1 ⇒ (15) 2x1 MUX Required.

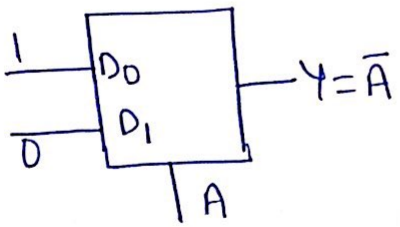
Similarly, ③ 256x1 MUX by 16x1 MUX

16	256
16	16
	1

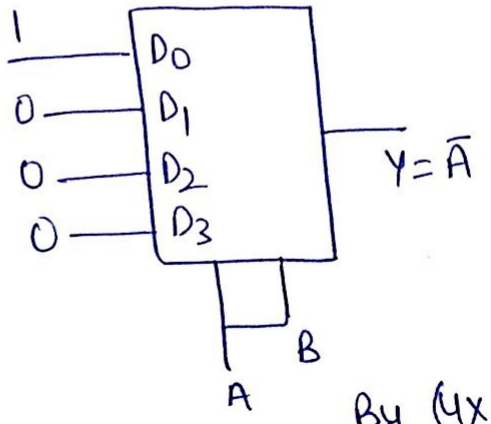
16+1 = (17) 16x1 MUX.

Implementation of Logic gates by using 2x1 MUX and 4x1 MUX:

① NOT gate:



By (2x1) MUX



By (4x1) MUX.

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Logic gate	2x1 MUX	4x1 MUX
NOT	1	1
AND	1	1
OR	1	1
NAND	2	1
NOR	2	1
EX-OR	2	1
EX-NOR	2	1

Combinational CKT	2x1 MUX	4x1 MUX
Half adder	2	
Half Subtractor	2	
Full Adder	7	3
Full subtractor	7	3
Comparator	3	

Que 2 For the implementation of AND gate & XOR gate the no. of MUX required:

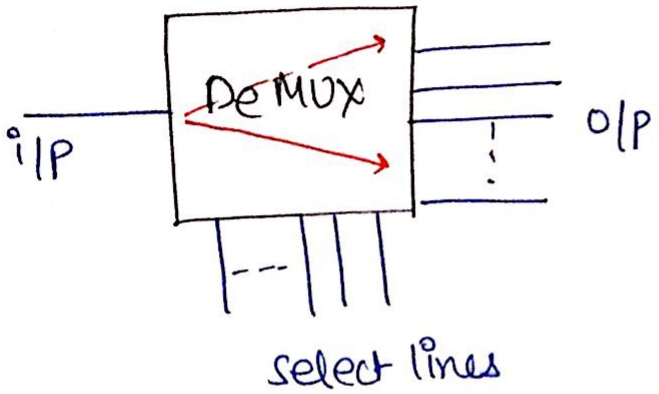
a) 1,1 b) 1,2 c) 2,1 d) 2,2

Soln. 1 MUX: AND , 2 MUX : XOR [B]

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→ Demultiplexer:

A deMUX performs the reverse operation of MUX.

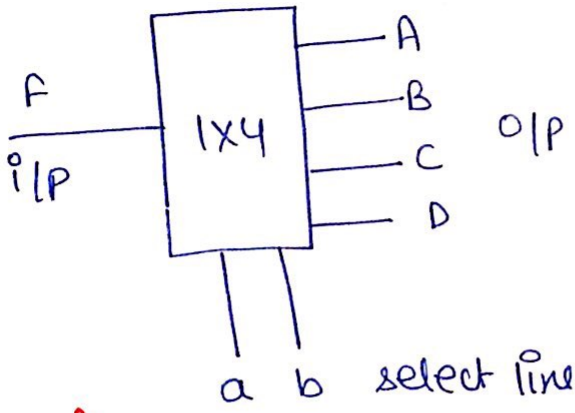


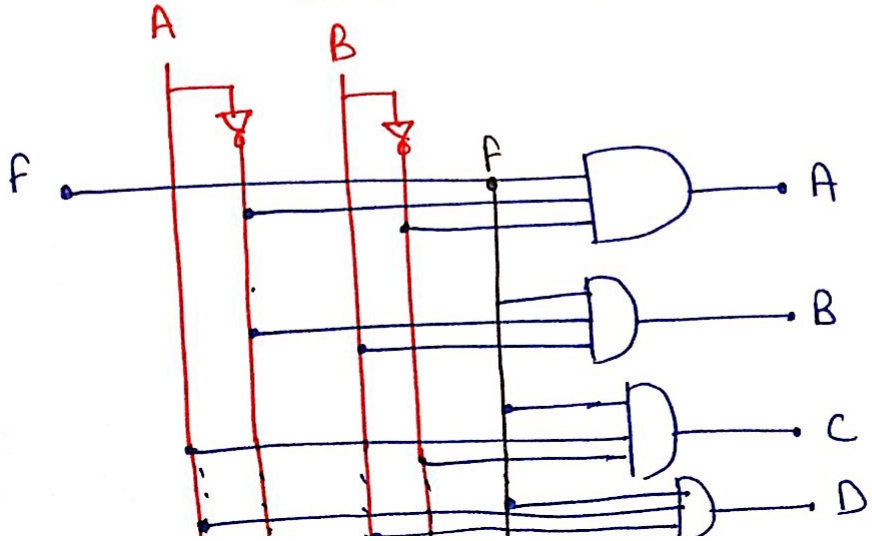
→ no. of outputs = 2^n where n → select lines

→ also ~~clas~~ called as data detector.

→ By setting the input to true (1), the demux behaves as decoder.

1X4 DeMUX:

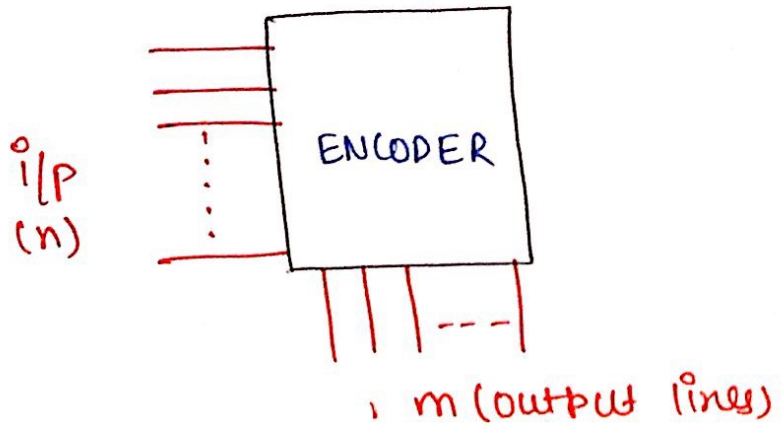




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→ Encoders:

An encoder converts an active input signal into a coded output signal.



→ At a time only one of the input lines is active.

→ interminal logic within the encoder converts this ~~bin~~ active line to a coded binary output with m bits.

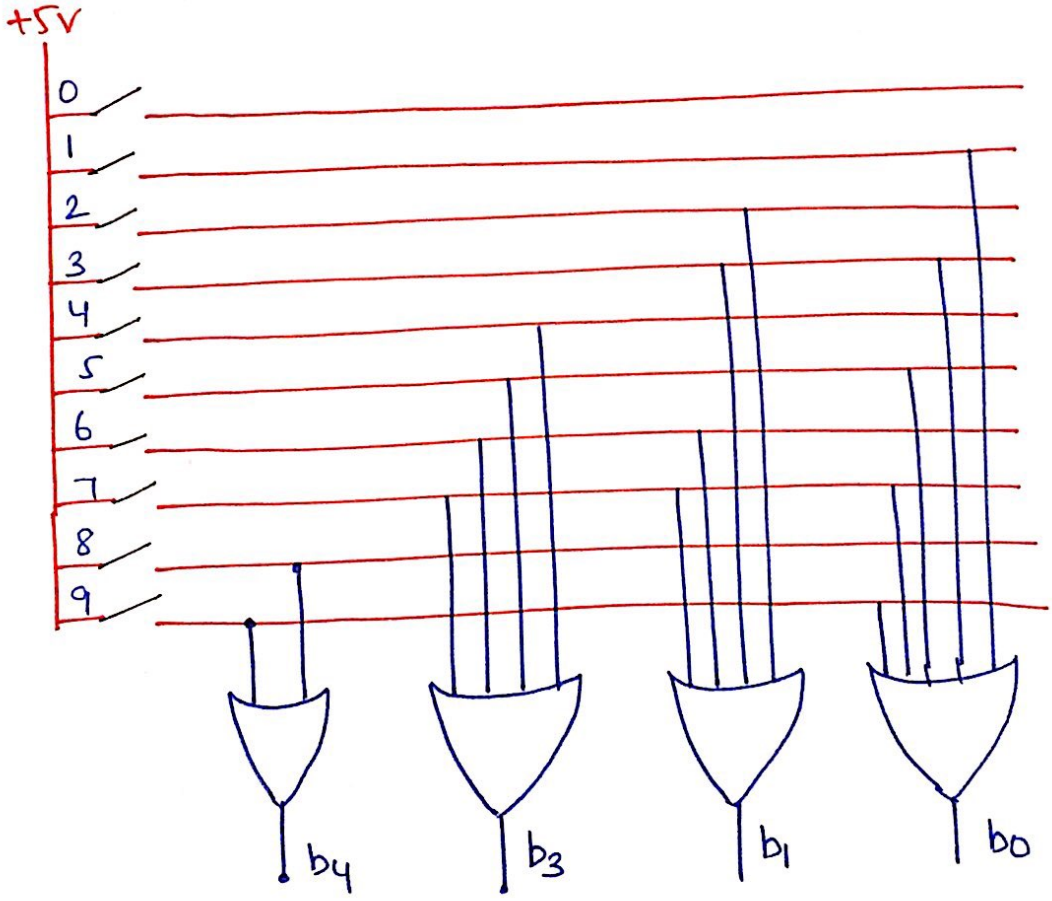


Fig: Decimal to BCD encoder.

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→ when switch T:

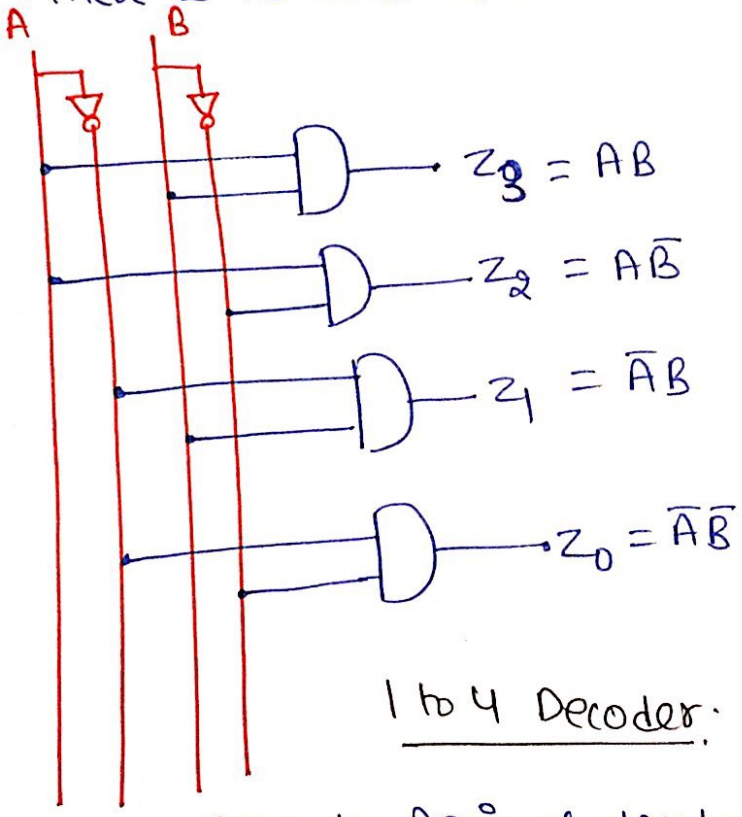
OR gates 3, 2, 1 are active
& gate 4 is inactive

b_4 b_3 b_2 b_1
(0 1 1 1) Ans.

→ Decoders:

→ A decoder decodes the coded input signal into an active O/P signal.

→ A decoder is similar to deMUX, with one exception: there is no data input.



1 to 4 Decoder.

BCD to Decimal decoder.

e.g. 1001 → Decimal equivalent = 9

*** → 2x4 decoder with enable input ≡ 1x4 deMUX.

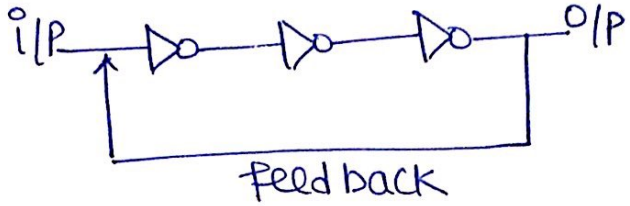
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SEQUENTIAL CIRCUIT

→ **FLIP-FLOP:**

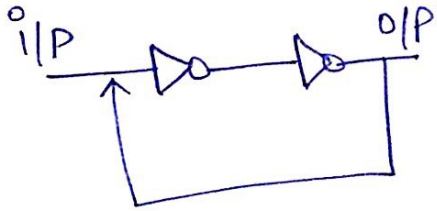
1) Basic memory element of Digital system.
2) FF can store 1-bit memory.
3) every FF will have two outputs (0 & 1) or ($Q, \overline{Q}$)
4) also called as bistable multivibrator.

Astable multivibrator: odd number of NOT gates with feedback.



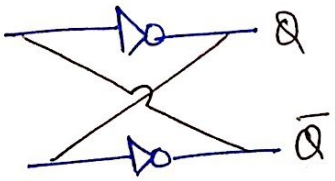
→ output changes each time, it is not a memory element.

Bistable multivibrator:



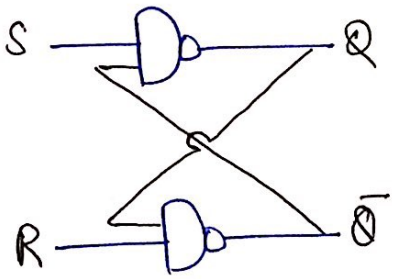
even no. of NOT gate with feedback.

latch:



use to store 1-bit memory.

→ Replace each not by NAND gate:



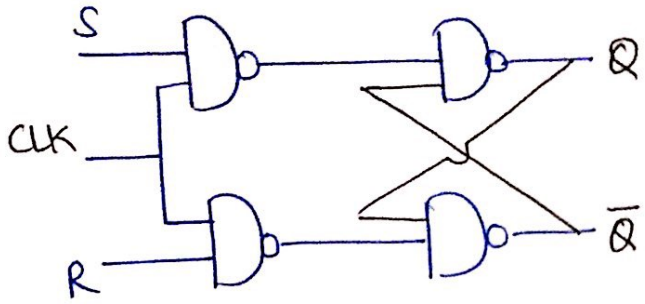
(S-R latch)

S	R	Q
0	0	invalid
0	1	1
1	0	0
1	1	Prev.

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① S-R Flip Flop:

S : Set = 1 ; R : Reset = 0



CLK	S	R	Q
0	X	X	Prev.
1	0	0	Prev.
	0	1	0
	1	0	1
	1	1	invalid.

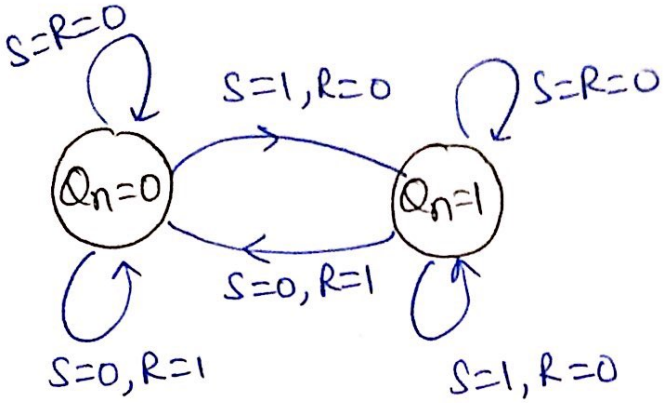
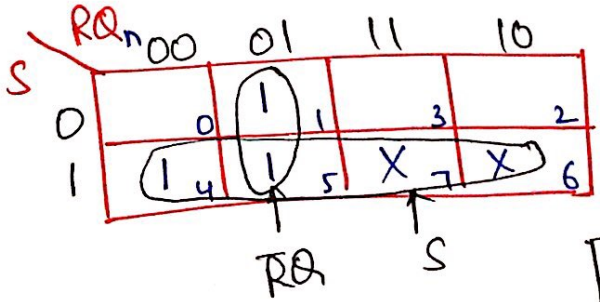


Fig: State transition Diagram.

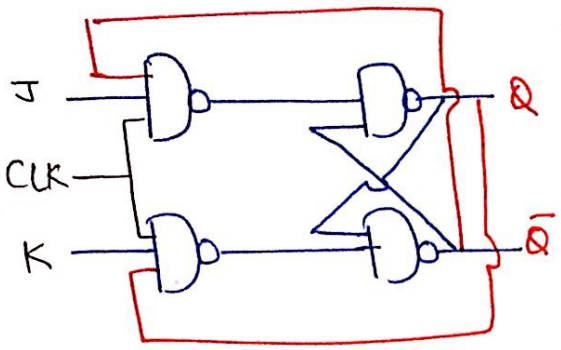
	S	R	Q	Q_{n+1}	
0⟩	0	0	0	0	(Prev.)
1⟩	0	0	1	1	
2⟩	0	ϕ	0	0	→ follows
3⟩	0	1	1	0	
4⟩	1	0	0	1	→ follows
5⟩	1	0	1	1	
6⟩	1	1	0	X	→ invalid.
7⟩	1	1	1	X	

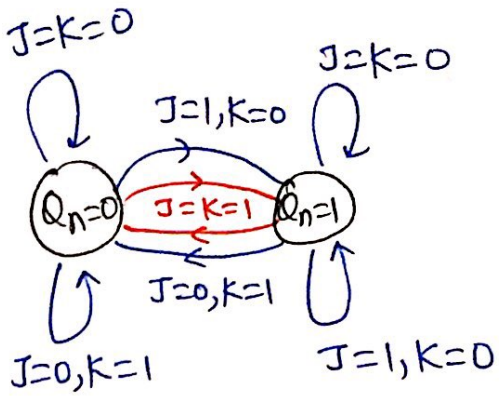


Ch. eqⁿ = $S + \bar{R}Q_n$

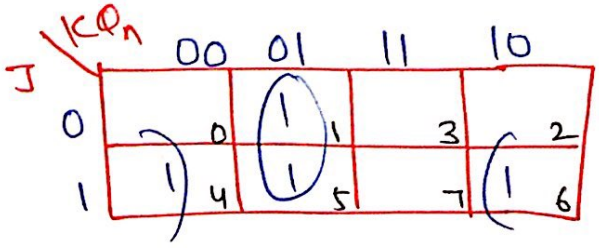
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② J-K Flip Flop:





J	K	Q_n	Q_{n+1}	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	



$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Edge triggered FF: o/p changes only at the edges either at +ve edge or at -ve edge.



level triggered FF: when clock is kept at proper level, any change in i/p will be observed at o/p.

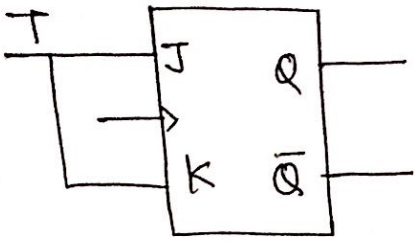
Race around condition: (J=K=1)
under single clock pulse o/p changes many times.

Removal: $t_{CLK} < t_{FF}$

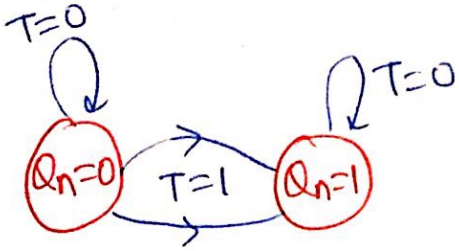
To achieve this cond^n, we use FF in cascade.

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③ T-flip flop:

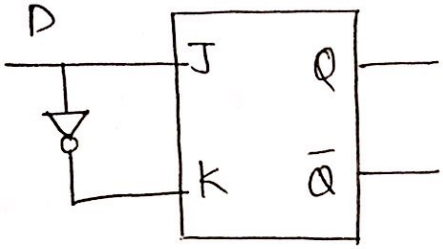


clk	T	Q_{n+1}
0	x	Previous
1	0	Previous
	1	$\bar{Q}_n$

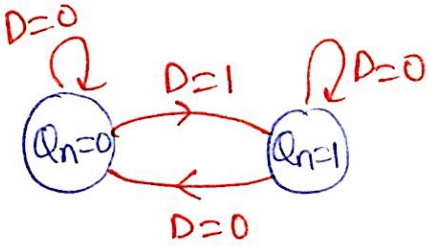


ch. eqn: $T \oplus Q_n$

④ D-flip flop: (transparent | Buffer | Delay FF)

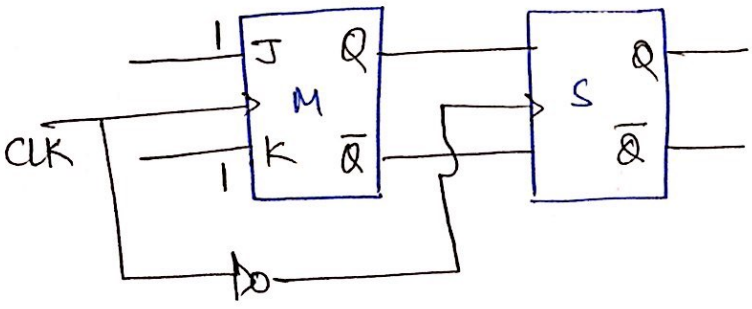


D	Q_{n+1}
0	Prev.
1	1



ch. eqn: $D = Q_{n+1}$

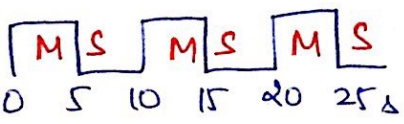
⑤ master-slave ff:



① O/P of master always toggles & behaves as i/p for slave

② i/p for slave never be 1,1 or 0,0 hence race around condn is removed.

Input :



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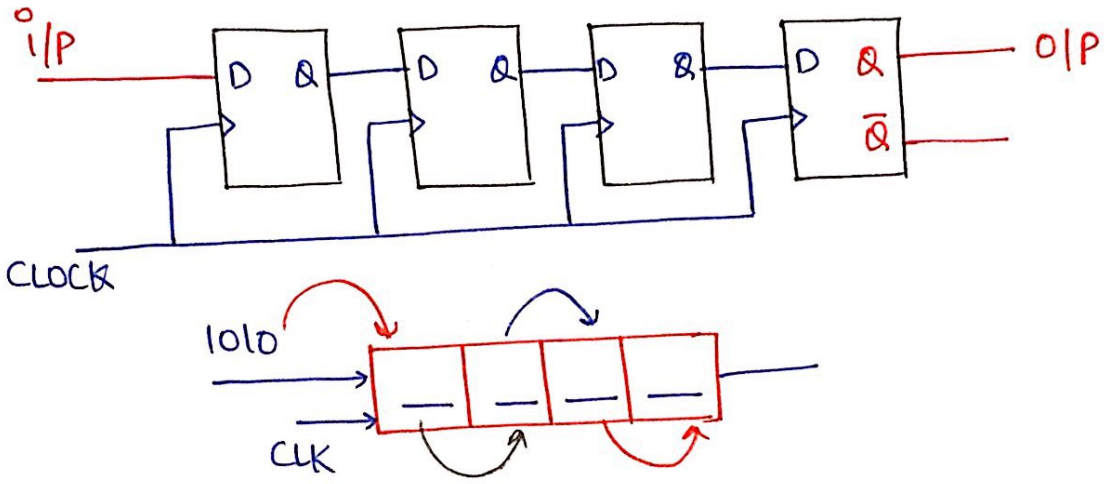
→ Registers:

1) mainly implemented by D flip-flop.
2) n ff are required to store n-bit data.
3) mainly of four types:

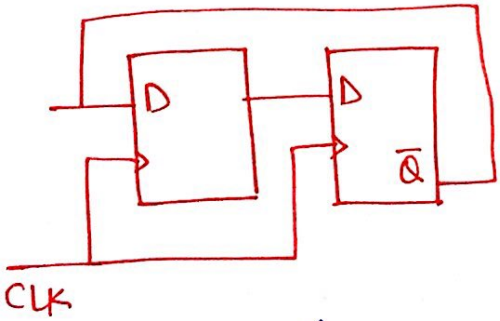
- SISO
- SIPO
- PISO
- PIPO

} based on i/p & o/p

Serial input series output Register:

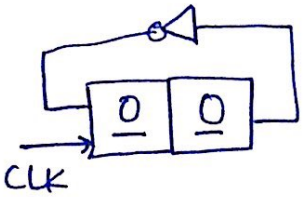


Que! Determine the content after 373 clock Pulse:



a) 10 b) 11
c) 01 d) 00

Sol^n:-



$\frac{373}{4} = 93\ \frac{1}{4}$

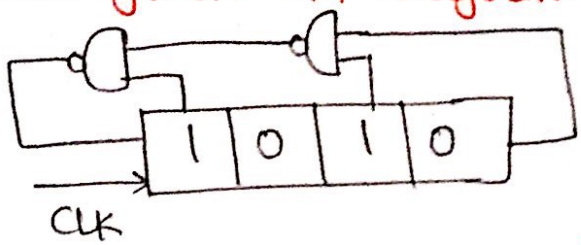
CLK	D_0	P_1
X	0	0
1)	1	0
2)	1	1
3)	0	1
4)	0	0

mod = 4

A

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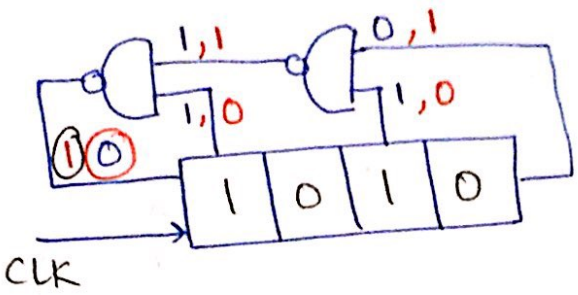
Que 2 For the given CKT diagram shown



Determine the content of Register after 3 clock Pulse?

a) 1010 b) 0101 c) 0110 d) 0111

Soln:-



CLK : A_0 A_1 A_2 A_3

x) 1 0 1 0

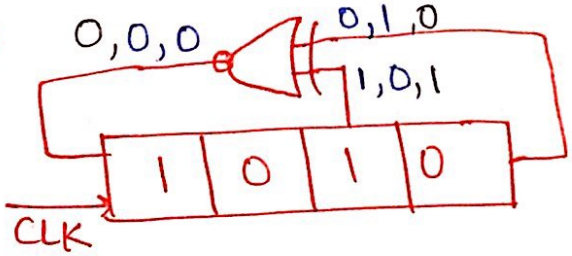
1) 0 1 0 1

2) 1 0 1 0

3) 0 1 0 1

B

Que 3 Determine the content of Register after 3rd clock Pulse:



Soln:-

CLK Q_0 Q_1 Q_2 Q_3

x) 1 0 1 0

1) 0 1 0 1

2) 0 0 1 0

3) 0 0 0 1

Ans.

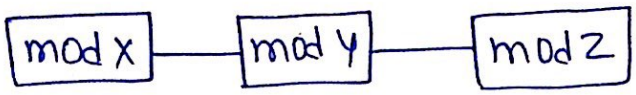
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→ COUNTERS:

modulus: total no. of distinct states.

e.g. mod-4 counter

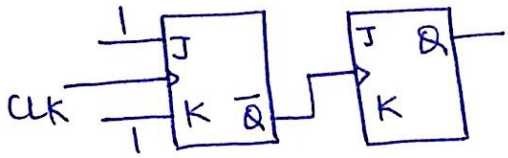
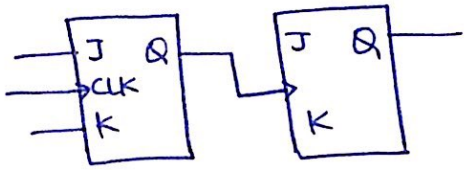
00, 01, 10, 11 → 4-states.



Total mode = X.Y.Z

1) Asynchronous counter (Ripple counter)

→ only J-K & T FF are used (J=K=1)

up counter	down counter
$\bar{Q}$ of first FF fed into clock of 2nd FF.	Q of first FF fed into clock of 2nd FF
	

→ 1st FF : LSB

LSB ⟶ MSB

⟵ To Read.

*** → mod = 2^n = no. of clock Pulse.

Qu! a mod-16 counter have initial state 0110. determine the count sequence after 37th Clock Pulse?

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Sol^{n}:- Initial : 0110

after 16 CLK : 0110

after 32 CLK : 0110

33 : 0111

34 : 1000

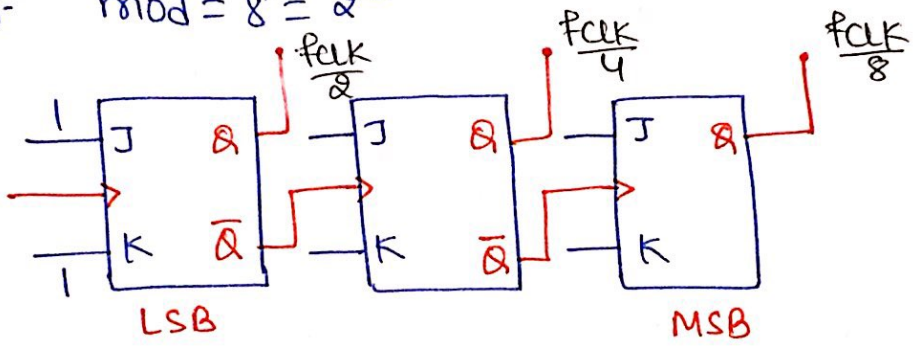
35 : 1001

36 : 1010

37 : (1011) Ans.

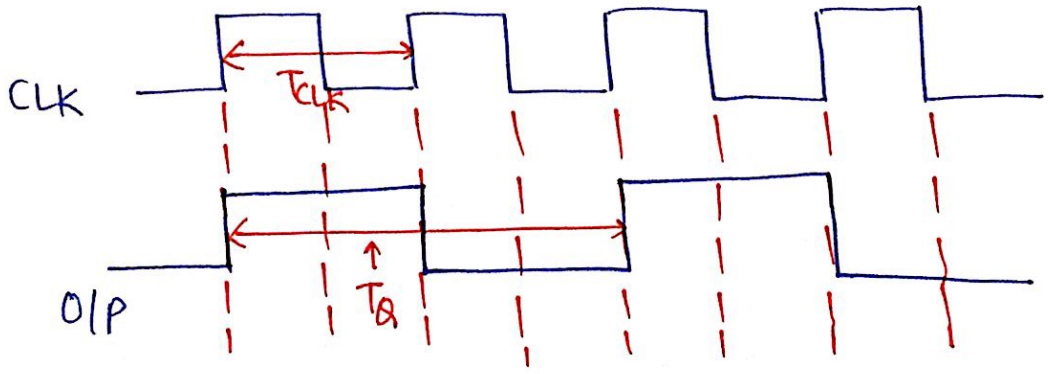
Que:- Design mode 8 up counter using +ve edge triggered flip flop?

Sol^{n}:- mod = 8 = 2^3



Time Period & Frequency:

For mod-2 counter.



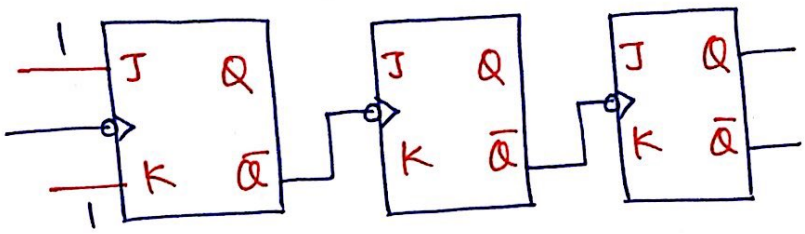
$T_Q = 2\,T_{CLK}$

$f_Q = \frac{1}{2T_{CLK}} = \frac{f_{CLK}}{2}$ i.e Freq. divider.

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Que 3 Design mod 8 down counter by using -ve edge triggered JK FF?

Soln:-



Reduction of States:

To reduce no. of states Preset & clear are used.

Preset: is used to display o/p = 1
Clear: is used to display o/p = 0
} → both have i/p = 1

Que 4 Design a mod 6 up counter by using -ve edge triggered JK FF?

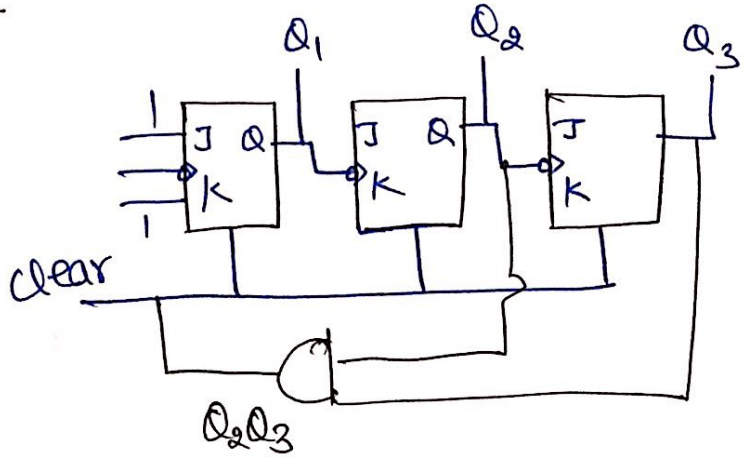
Soln:- $2^2 < 6 < 2^3 \Rightarrow n = 3$

Q_3	Q_2	Q_1	clear
0	0	0	
0	0	1	
0	1	0	
0	1	1	0
1	0	0	
1	0	1	
1	1	0	1
1	1	1	1

$CL = Q_3 Q_2 \bar{Q}_1 + Q_3 Q_2 Q_1$

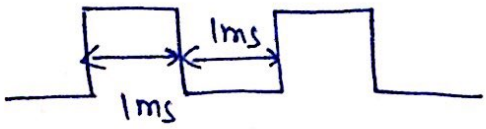
$CL = Q_3 Q_2$

↑ AND gate.



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Duty cycle:



$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON}+T_{OFF}} \Rightarrow \frac{1ms}{1ms+1ms} = 50\%.$$

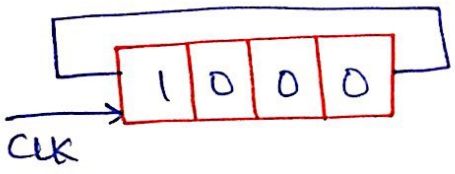
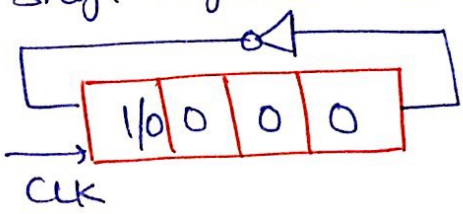
Time delay:

$$T = n \times t_{pd\,FF} + t_{Pd\,gate}$$

2) Asynchronous counter:

→ all FF's can be used

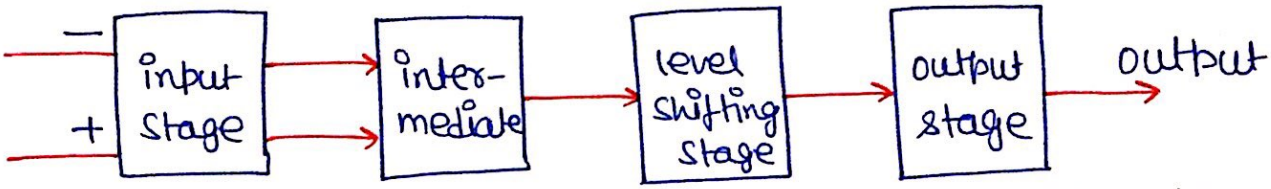
→ single clock is fed to all FF's.

RING counter	Johnson Counter
Shift Reg. + feedback 	Shift Register + $\overline{Q}$ 
mod = no. of FF used state = n waste = $2^n - n$	mod = 2 (no. of FF) used state = 2n waste = $2^n - 2n$
$f_{CLK} = n \times f_Q$ $f_Q = \frac{f_{CLK}}{n}$	$f_{CLK} = 2n \times f_Q$ $f_Q = \frac{f_{CLK}}{2n}$

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OPERATIONAL AMPLIFIER

Block Diagram:



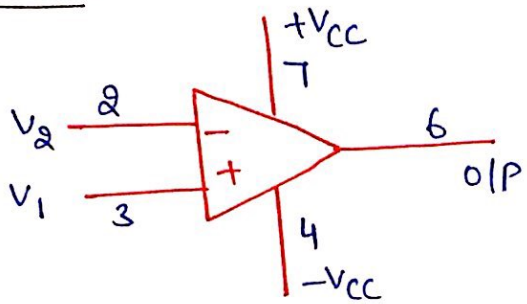
Dual i/p Balanced o/p Diff. Amp. → to ↑ CMRR

Dual i/p unbalanced o/p Diff. Amplifier → ↑es gain

Emitter follower with constant current source

complementary symmetry Pull-Push amplifier. → ↑es o/p voltage

Symbol:

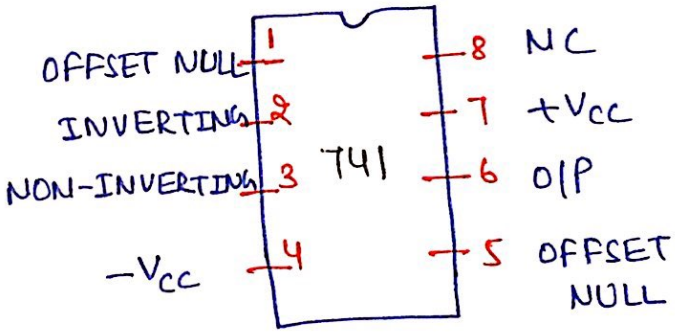


$V_{in} = V_1 - V_2$

$V_0 = A V_{in}$

$\boxed{V_0 = A(V_1 - V_2)}$

Fig: IC 741



Power supply:



Common Chassis Earth

→ Ideal OP-Amp:

1) open loop gain: $A = \infty$
2) input Resistance: $R_{in} = \infty$
3) output Resistance: $R_0 = 0$
4) Perfect balance
5) ∞ frequency band width
6) CMRR $= \infty$
7) Slew Rate $= \infty$
8) offset voltage $= 0$
9) voltage controlled voltage source

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$V_{out} = A(V_1 - V_2) = \infty$

non-inverting	Buffer	Inverting
$V_1 > V_2$	$V_1 = V_2$	$V_1 < V_2$
$V = +\infty$	$V =$ undefined	$V = -\infty$

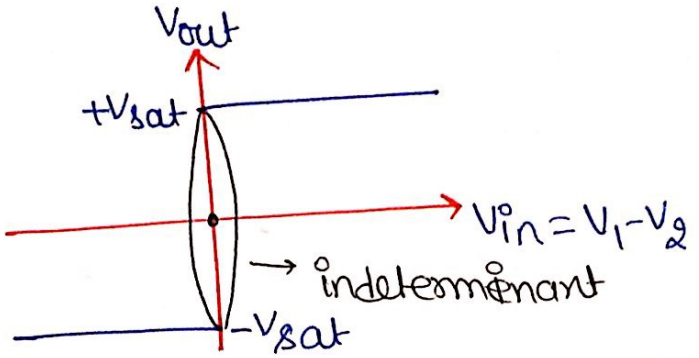
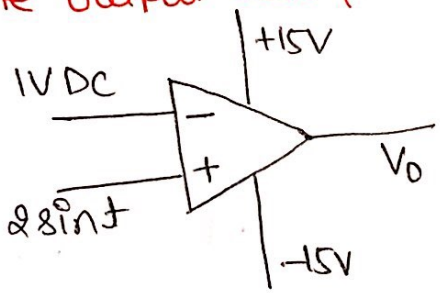
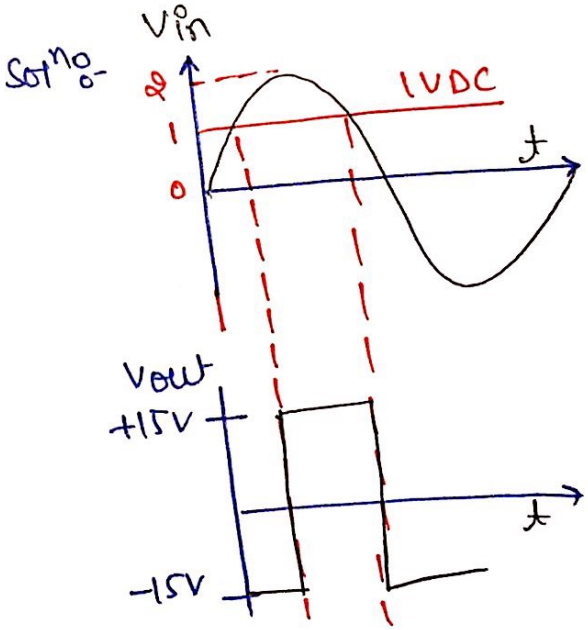


Fig: ideal Transfer characteristics

Que! For the given circuit diagram shown, sketch the output waveform





→ CMRR:

Common mode Rejection Ratio.

→ ability to cancel out certain types of undesired voltage signals e.g noise.

$$CMRR = \frac{A_d}{A_{cm}}$$

$$A_d = \frac{A_1 - A_2}{2}$$

$$A_{cm} = (A_1 + A_2)$$

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$V_d = V_1 - V_2$ & $V_{cm} = \frac{1}{2}(V_1 + V_2)$

$V_{out} = A_d V_d + A_{cm} V_{cm}$

CMRR in dB $= 20 \log_{10}\left(\frac{A_d}{A_{cm}}\right)$ → in terms of voltage

$= 10 \log_{10}\left(\frac{A_d}{A_{cm}}\right)$ → in terms of Power.

Que 2 A differential amplifier has a differential gain of 20,000 ; CMRR = 80dB. The common mode gain is given by :

a) 2 b) 1 c) 0.5 d) 0

Soln :- $80\,dB = 20 \log\left(\frac{A_d}{A_c}\right)$

$\log(A_d/A_c) = 4\,dB$

$\frac{A_d}{A_c} = 10^4 \Rightarrow A_c = \frac{A_d}{10^4} = \frac{20,000}{10,000}$

$\boxed{A_c = 2}$ **A**

Que 3 A power amplifier gives 150 w output for an input of 1.5 w. The gain in dB is :

a) 10 b) 20 c) 54 d) 100

Soln :- $A_d = \frac{150w}{1.5w} = 100$

gain in dB $= 10 \log_{10}(10)^2$ **B**

$= 20 \log_{10}(1) = 20\,dB$

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Ques A differential dc amplifier has a differential mode of gain of 100 & a common mode gain 0.01. what is its CMMR in dB?

a) 20 b) 40 c) 60 d) 80

Soln:- CMRR in dB = $20 \log_{10}\left(\frac{A_d}{A_c}\right)$

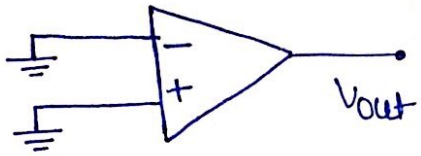
$= 20 \log_{10}\left(\frac{100}{0.01}\right)$ D

$= 20 \log_{10} 10^4 = 80$ dB

→ Practical OP-AMP Parameters:

1) DC characteristics:

a) Input offset voltage:



To cancel o/p offset voltage some i/p is applied, called i/p offset voltage.

b) output offset voltage: when no input is applied, some output is present, is called output offset voltage

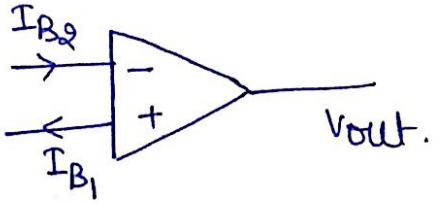
c) Input Bias current:

$$I_B = \frac{I_{B_1} + I_{B_2}}{2}$$

I_{B_1} & I_{B_2} → current in each input.

d) Input offset current:

$$I_{in(offset)} = I_{B_1} - I_{B_2}$$



e) Thermal drift.

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2) AC characteristics:

a) Gain Bandwidth Product (GBW)

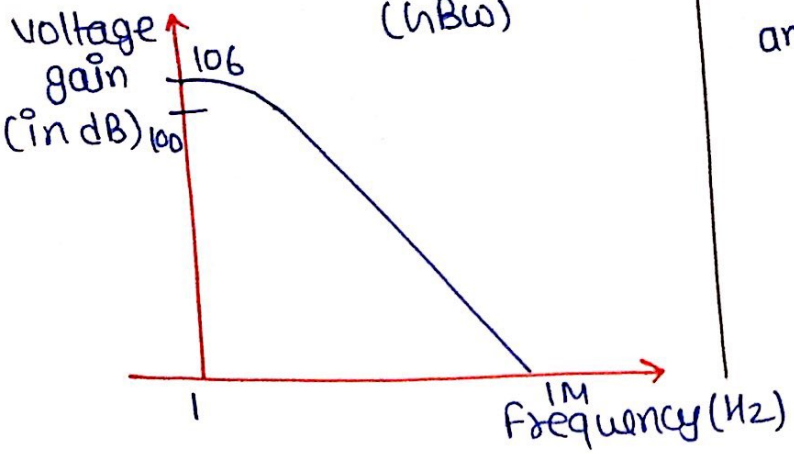
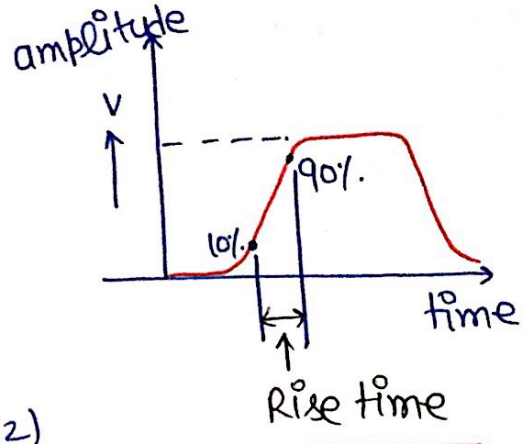


Fig: Open loop freq. Response of 741 C

$$GBW = A_{closed} \times f_H$$

b) Rise time:



$$t_{Rise} = \frac{0.35}{f_H}$$

c) Slew rate:

It represents How Fast OP-AMP operates. ***

$$SR = \left.\frac{dV_o}{dt}\right|_{max}$$

Slew Rate eqn:

$V_{in} = V_{pin} \sin \omega t$ & $V_o = V_{Pout} \sin \omega t$

$$SR = 2\pi f V_{Pout} \quad V/s$$

d) Power supply Rejection Ratio (PSRR):

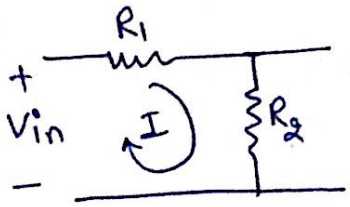
$$PSRR = \frac{\text{Change in i/p offset voltage}}{\text{Change in supply voltage}}$$

e) Full Power Response:

$$f_{max} = \frac{SR_{max}}{2\pi V_{Pout}}$$

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Voltage Division Rule:



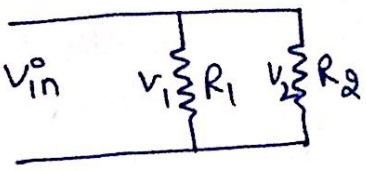
$$-V + I_1R_1 + I_2R_2 = 0$$

$$V = I(R_1+R_2)$$

$$I = \left(\frac{V}{R_1+R_2}\right)$$

$$\boxed{V_2 = IR_2 = \left(\frac{V}{R_1+R_2}\right)R_2}$$

Current Division Rule:



$$V_1 = V_2$$

$$I_1R_1 = I_2R_2$$

$$I_1 = \left(\frac{R_2}{R_1}\right)I_2$$

$$I = I_1 + I_2 = \frac{I_2R_2}{R_1} + I_2$$

$$I = I_2\left(\frac{R_1+R_2}{R_1}\right)$$

$$\boxed{I_2 = \left(\frac{I}{R_1+R_2}\right)R_1}$$



L (Henery) → SI

$R = j\omega L$ → Ohm

for dc : $R = 0\Omega$



Short CKT



$$R = \frac{1}{j\omega C} \text{ (ohm)}$$

for dc: $R = \frac{1}{0} = \infty$



Open CKT.

Closed loop OP-AMP:

→ OP-AMP that uses feedback

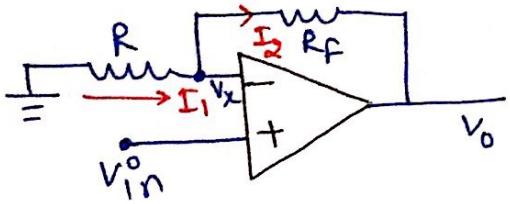
→ types:

1) voltage series feedback (closed loop non inverting) amplifier
2) voltage shunt feedback (closed loop inverting) amplifier
3) Differential amplifier.

→ inverting & non-inverting terminals are virtually connected.

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1) Non-inverting OP-AMP:



due to virtual ground concept:

$V_{in} = V_x$

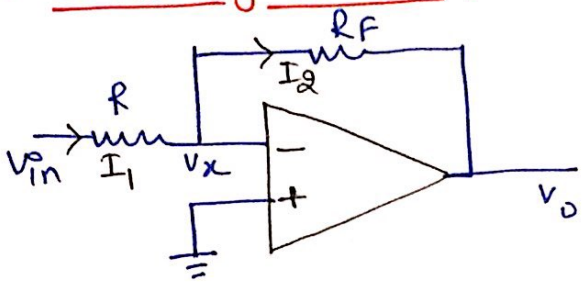
$I_1 = I_2$

$$\frac{0 - V_{in}}{R} = \frac{V_{in} - V_o}{R_f}$$

$\Rightarrow$ gain $= A_f$

$$\frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R}\right)$$

2) Inverting OP-AMP:



$V_x = 0$ (virtual ground concept)

$I_1 = I_2$

$$\frac{V_{in} - V_x}{R} = \frac{V_x - V_o}{R_f}$$

$$\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

→ Closed loop voltage gain:

$$A_f = \frac{V_o}{V_{in}} = \frac{A}{1 + A\beta}$$

$\beta \rightarrow$ feed back factor.

→ Input impedence of Amplifier:

N-inverting.	inverting
$Z_{in} = R_{in}(1 + A\beta)$	$Z_{in} = R_{in}$

A → open loop gain

$$A = \frac{V_o}{V_d}$$

→ Output impedence of Amplifier:

$$Z_{out} = \frac{R_{out}}{1 + A\beta}$$

$$\beta = \frac{R}{R + R_f}$$

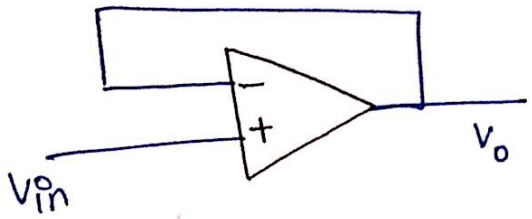
→ Band width with feed back:

$$f_f = f_o(1 + A\beta)$$

$$A_f = \frac{V_o}{V_{in}}$$

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3) Voltage Follower:



$$V_{out} = V_{in}$$

$$A_f = 1$$

$$\frac{V_o}{V_{in}} = \frac{A}{1+A\beta}$$

$$\beta = 1$$

$$\frac{V_o}{V_{in}} = \frac{A}{1+A} = 1$$

for $A \gg 1$

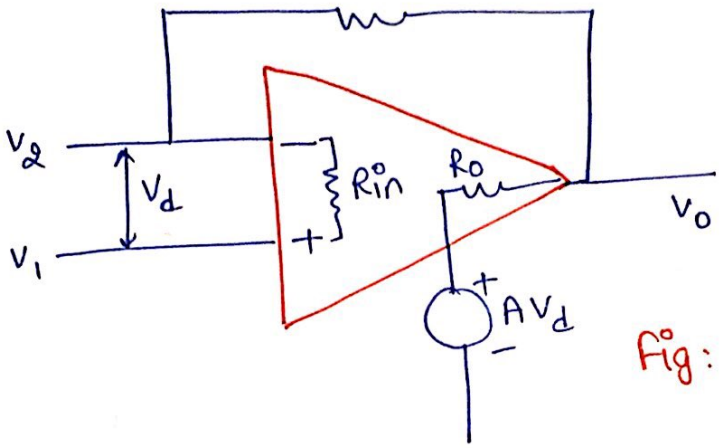
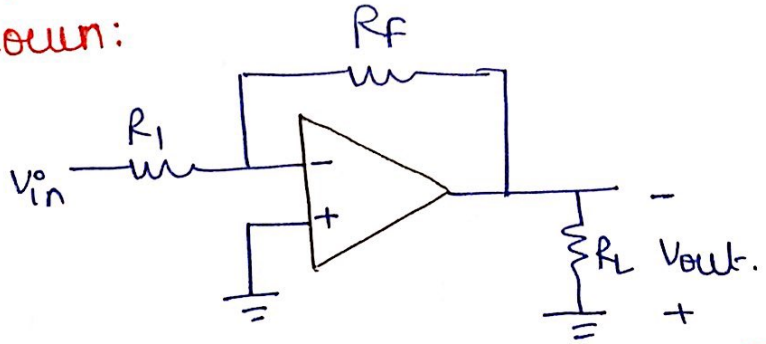


Fig: internal diagram of OP-AMP.

Que! Determine the voltage gain, input resistance, output resistance and bandwidth for the CKT shown:



If $R_1 = 330\Omega$ & $R_f = 3.3K\Omega$. $A = 2\times10^5$, $R_{in} = 2M\Omega$, $R_{out} = 75\Omega$ and $f_0 = 5$ Hz.

Soln:- feedback factor $(\beta) = \frac{R_1}{R_1+R_f} = \frac{330}{330+3300} = \frac{1}{11}$

$$(1+A\beta) = 1 + \left(2\times10^5 \times \frac{1}{11}\right) = 18,182.8$$

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Closed loop gain: $A_f = -\frac{R_f}{R_1} = -\frac{3300}{330} \Rightarrow -10$

$Z_{in} = R_1 = 330\Omega$

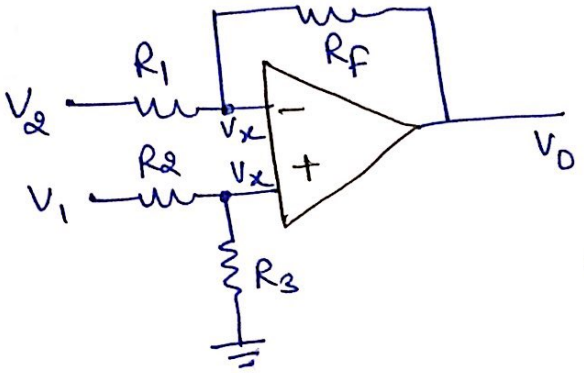
$Z_{out} = \frac{R_{out}}{1+A\beta} = \frac{75}{18182.8} \Rightarrow 0.00412\Omega$

$f_f = f_0(1+A\beta) = 5 \times 18182.8$

$= 90.92$ KHz

4) Differential Amplifier:

used to amplify the difference b/w two signals.



$V_x = \left(\frac{V_1}{R_2+R_3}\right) R_3$

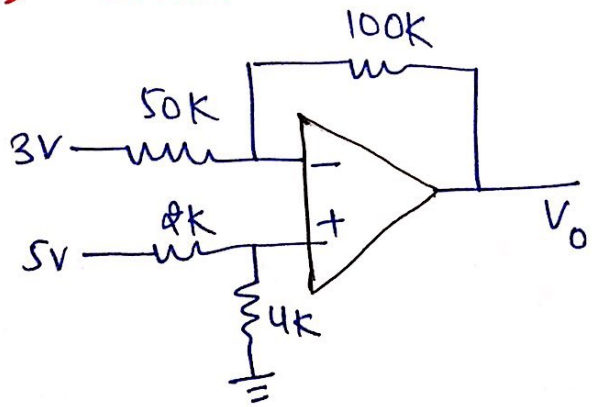
$V_0 = A_d(V_1 - V_2)$

$\boxed{V_0 = A_d V_d}$

Condn:

If, $\frac{R_1}{R_f} = \frac{R_2}{R_3}$ then $\boxed{V_0 = V_d \times \frac{R_f}{R_1}}$

Que Determine the output (V_0) of the given circuit:



$V_d = (5-3) = 2V$

Soln: $\frac{R_1}{R_f} = \frac{R_2}{R_3}$

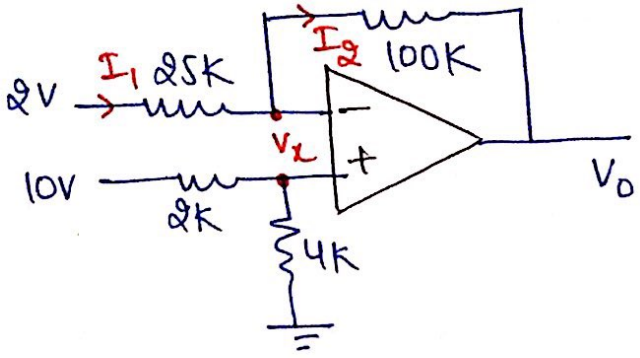
$\frac{50}{100} = \frac{2}{4}$

$V_0 = V_d \times \frac{R_f}{R_1} = 2V \times \frac{100}{50}$

$\boxed{V_0 = 4V}$

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Que 3 Determine the output of the given circuit: (5)



$$\frac{R_f}{R_1} \neq \frac{R_3}{R_2}$$

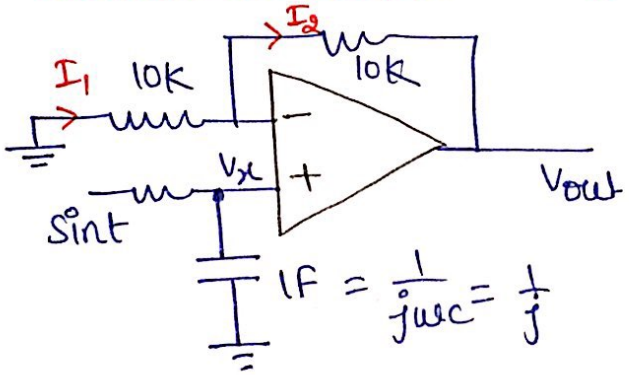
Soln:- $$V_x = \left(\frac{10V}{2K+4K}\right) \times 4K = \frac{20}{3}V$$

now $I_1 = I_2$

$$\frac{2V - V_x}{25K} = \frac{V_x - V_{out}}{100K} \Rightarrow \boxed{V_{out} = \frac{76}{3}V}$$

Que 4 Determine output voltage of given circuit:

given: $\omega = 1, C = 1$



Soln:- $$V_x = \frac{\sin t}{1 + \frac{1}{j}} \times \frac{1}{j} = \frac{\sin t}{1+j}$$

now $I_1 = I_2$

$$\frac{0 - V_x}{10K} = \frac{V_x - V_{out}}{10K} \Rightarrow V_{out} = 2V_x$$

$$V_{out} = \frac{2\sin t}{1+j}$$

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$$V_{out}(mag.) = \frac{2\sin t}{\sqrt{1^2+1^2}} = \sqrt{2}\sin t$$

Phase angle:

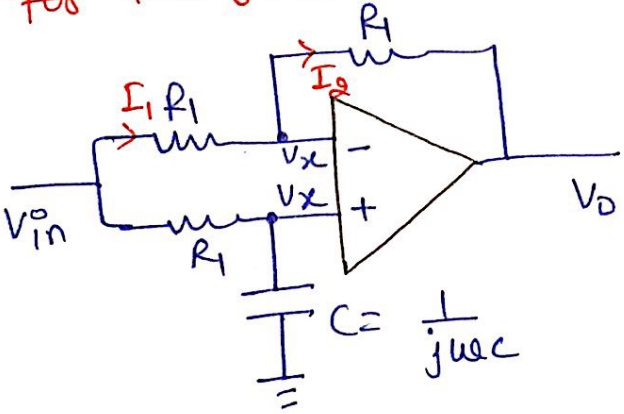
$$\theta = \frac{2\sin t}{1+j} = \underset{\downarrow 0}{\angle 2} * \underset{\downarrow 0}{\sin t} * \frac{1}{1+j}$$

$$\theta = \underset{\uparrow 0}{\angle 1} - \angle 1+j = -\tan^{-1}\left(\frac{b}{a}\right) = -\tan^{-1}\left(\frac{1}{1}\right)$$

$$\theta = -45^\circ$$

$$\boxed{V_{out} = \sqrt{2}\sin(t-45^\circ)}$$

Ques Determine the maximum phase shift of gain for the given circuit:



$$V_x = \frac{V_{in}}{R_1 + \frac{1}{j\omega c}} \times \frac{1}{j\omega c}$$

$$V_x = \frac{V_{in}}{1+j\omega R_1 C}$$

now $I_1 = I_2$

$$\frac{V_{in} - V_x}{R_1} = \frac{V_x - V_o}{R_1} \Rightarrow V_o = 2V_x - V_{in}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{1-j\omega R_1 C}{1+j\omega R_1 C}}$$

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Phase angle:

$$\angle\frac{V_o}{V_{in}} = \angle(1+j(\omega R_1 C) - \angle(1+j(\omega R_1 C))$$

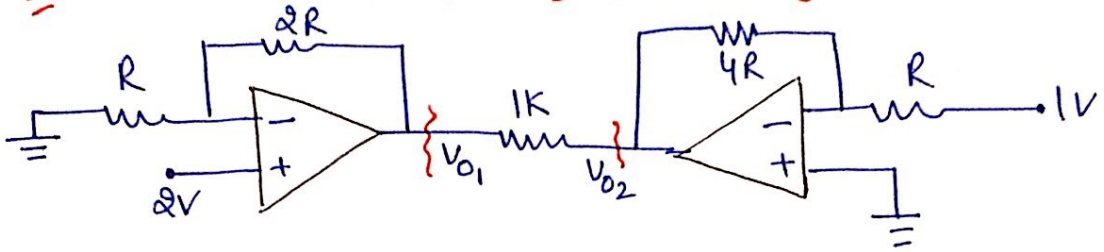
$$= \tan^{-1}\left(\frac{-\omega R_1 C}{1}\right) - \tan^{-1}\left(\frac{\omega R_1 C}{1}\right)$$

$$= -2\tan^{-1}\omega R_1 C$$

max Phase shift $\omega R_1 C \to \infty$

$$\theta = \pm 2 \times 90^\circ = \pm 180^\circ$$

Qu 6 Determine V_o & I_o for the given circuit:



a) 10V, 10mA b) 8V, 10mA c) 5V, 5mA d) 8V, 8mA

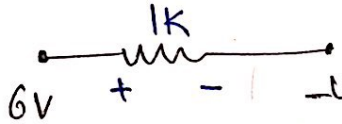
Soln:-

$$\frac{V_{o_1}}{V_{in}} = 1 + \frac{R_f}{R_1} \rightarrow \text{for non-Inverting OP-AMP}$$

$$V_{o_1} = \left(1+\frac{2R}{R}\right)V_{in} = (1+2)\times 2 = 6V$$

$$\frac{V_{o_2}}{V_{in}} = -\frac{R_f}{R_1} \rightarrow \text{for inverting OP-AMP}$$

$$V_{o_2} = \left(\frac{-4R}{R}\right)V_{in} = -4V$$



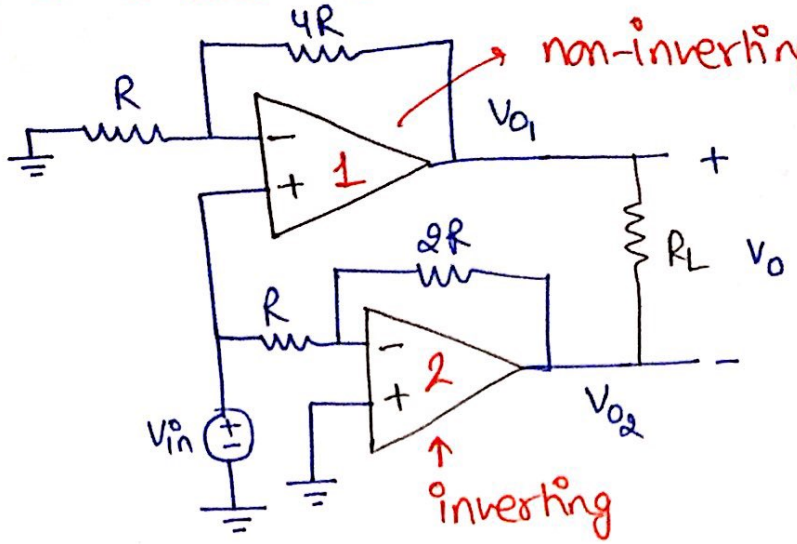
$$V_o = V_{o_1} - V_{o_2}$$

$$V_o = 6-(-4) = 10V$$

current: $I_o = \frac{V_o}{R_o} = \frac{10V}{1K} = 10mA$

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Que7 Determine output voltage and gain of the given circuit below:



Soln:- for OP-AMP 1:

$$\frac{V_{o_1}}{V_{in}} = 1 + \frac{R_f}{R_1}$$

$$= 1 + \frac{4R}{R} = 5$$

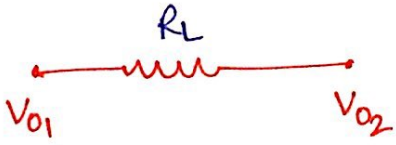
$$V_{o_1} = 5V_{in}$$

for OP-AMP 2:

$$\frac{V_{o_2}}{V_{in}} = -\frac{R_f}{R_1}$$

$$= -\frac{2R}{R} = -2$$

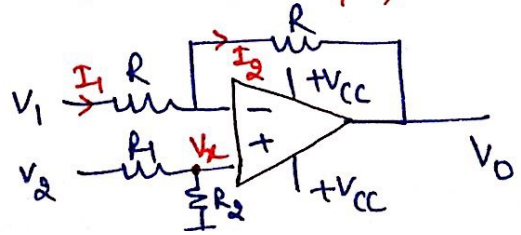
$$V_{o_2} = -2V_{in}$$



$$V_o = V_{o_1} - V_{o_2} = (5+2)V_{in} = 7V_{in}$$

$$\frac{V_o}{V_{in}} = 7$$

Que8 In the following circuit, for the output voltage to $V_o = (-V_1 + V_2/2)$ the ratio R_1/R_2 is:



a) 1/2 b) 1

c) 2 d) 3

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Soln:-

$$V_x = \left(\frac{V_2}{R_1+R_2}\right) R_2$$

now $I_1 = I_2$

$$V_x = \left(\frac{V_2}{R_1+R_2}\right) R_2$$

$$\frac{V_1 - V_x}{R} = \frac{V_x - V_{out}}{R}$$

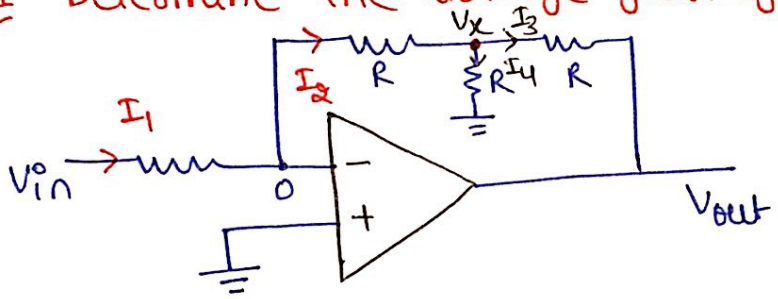
$$V_{out} = 2V_x - V_1 = -V_1 + \frac{V_2}{2} \text{ (given)}$$

$$2V_x = \frac{V_2}{2}$$

$$2\left(\frac{R_2}{R_1+R_2}\right)V_2 = \frac{V_2}{2}$$

$$\Rightarrow \boxed{R_1/R_2 = 3}$$

Que 9 Determine the voltage gain of the given circuit:



Soln:- $I_2 = I_3 + I_4$

$$\frac{0 - V_x}{R} = \frac{V_x - 0}{R} + \frac{V_x - V_0}{R}$$

$$-V_x = 2V_x - V_0$$

$$V_0 = 3V_x \quad -(1)$$

now, $I_1 = I_2$

$$\frac{V_{in} - 0}{R} = \frac{0 - V_x}{R}$$

$$V_{in} = -V_x \quad -(2)$$

Divide eqn (1) & (2)

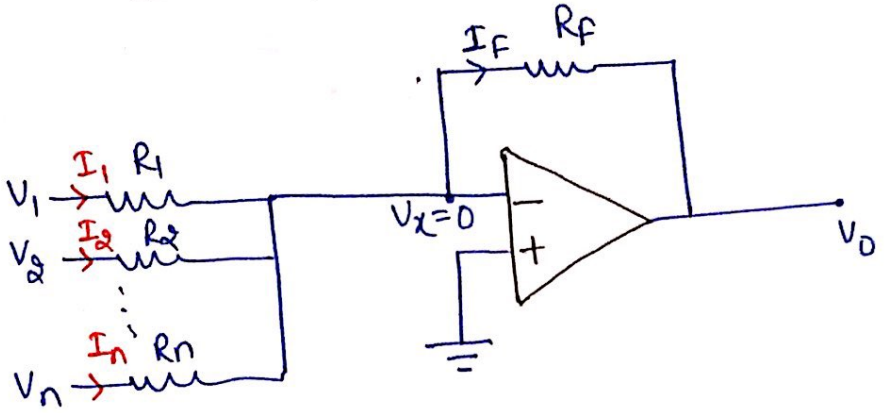
$$\frac{V_0}{V_{in}} = -\frac{3V_x}{V_x} = \boxed{-3}$$

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APPLICATIONS OF OP-AMPS

→ Summing Amplifier:

① Inverting Summing Amplifier:



$$I_F = I_1 + I_2 + \cdots\cdots + I_n$$

$$\frac{0-V_o}{R_f} = \frac{V_1-0}{R_1} + \frac{V_2-0}{R_2} + \cdots\cdots + \frac{V_n-0}{R_n}$$

If $R_1 = R_2 = \cdots = R_n = R$

$$\boxed{V_o = -\frac{R_f}{R}(V_1+V_2+\cdots+V_n)}$$

example: For an inverting summing amplifier, the magnitude of output voltage is:

$$|V_o| = 4V_1 + 6V_2 + 8V_3 \quad \text{—①}$$

If the value of feedback resistor is 10kΩ. Then determine the individual value of R_1, R_2 & R_3?

Soln:- $V_o = -\frac{R_f}{R_1}(V_1+V_2+V_3)$

$$|V_o| = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 \quad \text{—②}$$

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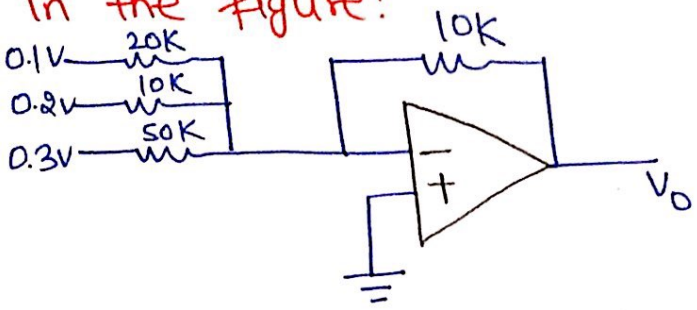
Compare eqn ① & ②

$$\frac{R_f}{R_1} = 4 \; ; \; \frac{R_f}{R_2} = 6 \; ; \; \frac{R_f}{R_3} = 2$$

$$R_f = 10K$$

$$R_1 = \frac{10}{4} = 2.5K \qquad R_2 = \frac{10}{6} = 1.6K \qquad R_3 = \frac{10}{2} = 5K$$

Example: Determine the V_{out} for the circuit shown in the figure:



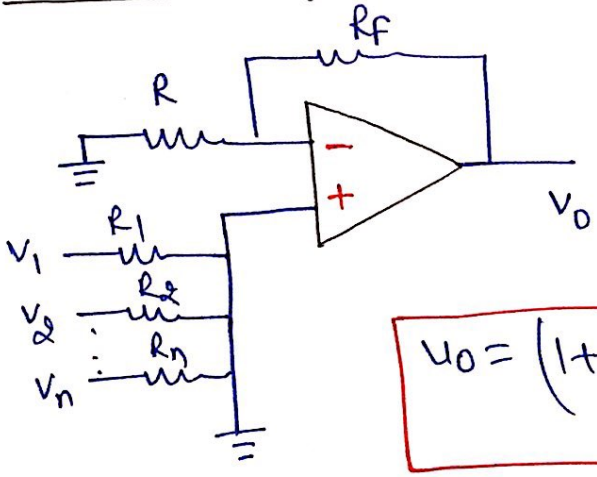
Soln$^{no}_{o}$-

$$V_{out} = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

$$= -10 \left[\frac{0.1}{20} + \frac{0.2}{10} + \frac{0.3}{50} \right]$$

$$= -0.31V$$

② Non-Inverting summing Amplifier:

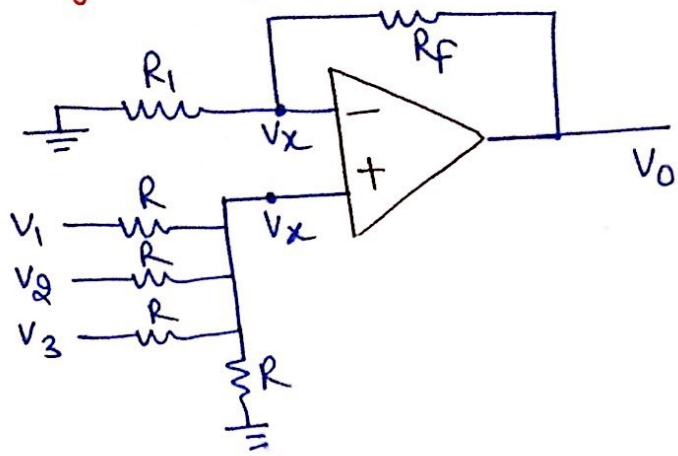


$$V_o = \left(1 + \frac{R_f}{R_1}\right) \left(\frac{V_1 + V_2 + \cdots}{n} \right)$$

n → no. of Resistors

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example: Determine the output voltage of the given circuit:

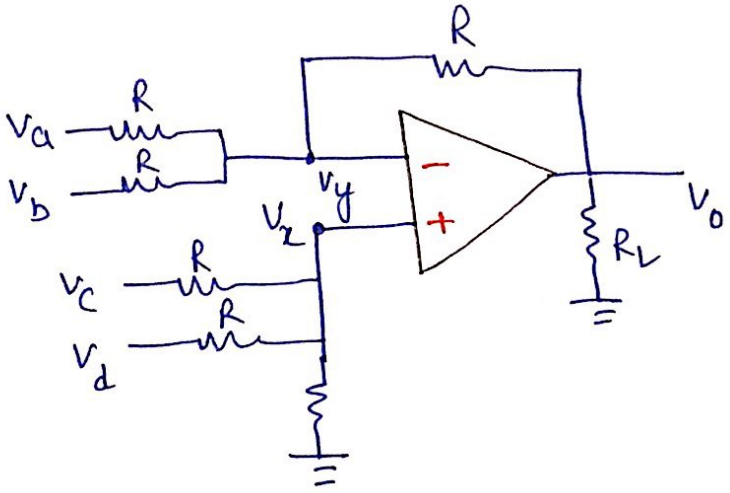


Soln:- $V_{out} = \left(1+\frac{R_f}{R_1}\right)\left(\frac{V_1+V_2+V_3}{n}\right)$

$n = 4$ (no. of resistors)

$$\boxed{V_{out} = \left(1+\frac{R_f}{R_1}\right)\left(\frac{V_1+V_2+V_3}{4}\right)}$$

③ Differential amplifier in summing configuration:



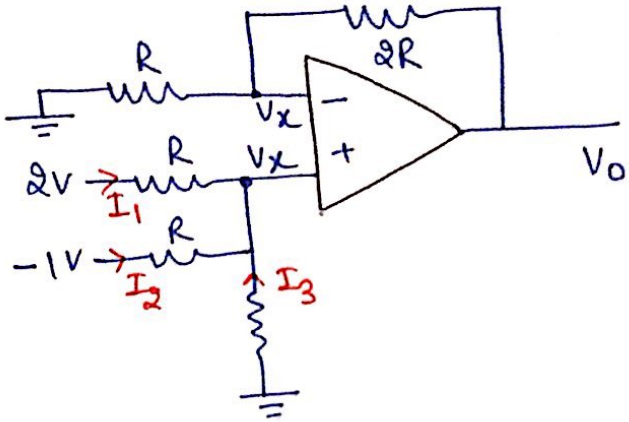
$$V_x = \frac{R/2}{R+R/2}V_c = \frac{V_c}{3}$$

$$V_{out_c} = \left(1+\frac{R}{R/2}\right)V_x = V_c \quad \text{similarly, } V_{out_d} = V_d$$

$$\boxed{V_{out} = -V_a - V_b + V_c + V_d}$$

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Example: For the figure shown below shows a noninverting OP-AMP summer with $V_1 = 2V$ & $V_2 = -1V$. The output voltage $V_o = ?$



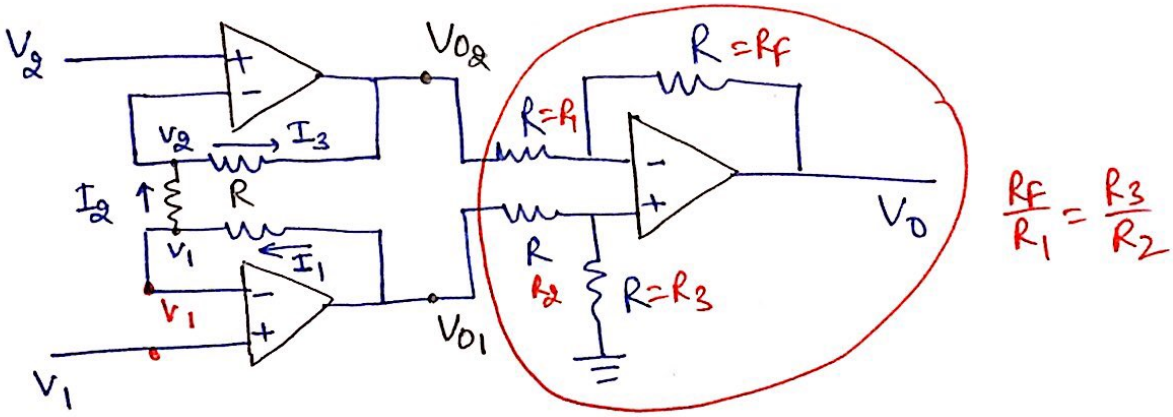
Soln:- $V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_1 + V_2}{n}\right)$

$= \left(1 + \frac{2R}{R}\right)\left(\frac{2V - 1V}{3}\right) \Rightarrow (1+2)\,1/3$

$= 1V$

④ Bridge Amplifier:

Example: Determine the output for the given OP-AMP:



$\frac{R_f}{R_1} = \frac{R_3}{R_2}$

Soln:- $I_1 = I_2$ | $I_2 = I_3$ | $V_o = V_d \times \frac{R_f}{R_1}$

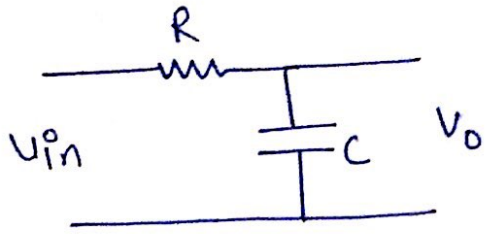
$\frac{V_o - V_1}{R} = \frac{V_1 - V_2}{R}$ | $\frac{V_1 - V_2}{R} = \frac{V_2 - V_{o2}}{R}$ | $V_o = 3(V_1 - V_2)$

$V_{o1} = 2V_1 - V_2$ | $V_{o2} = 2V_2 - V_1$ | $\frac{V}{V_1 - V_2} = 3$

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→ **FILTERS:**

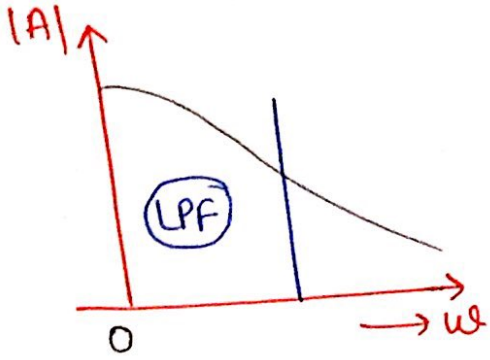
① **Low Pass Filter (LPF):**



$$V_o = \left(\frac{V_{in}}{R+\frac{1}{j\omega C}}\right)\frac{1}{j\omega C}$$

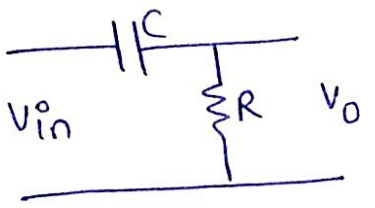
$$\frac{V_o}{V_{in}} = \frac{1}{1+j\omega RC}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\sqrt{1^2+\omega^2R^2C^2}}$$



i.e gain is high at low ~~frequencies~~. Hence, called LPF. example: Integrator CKT.

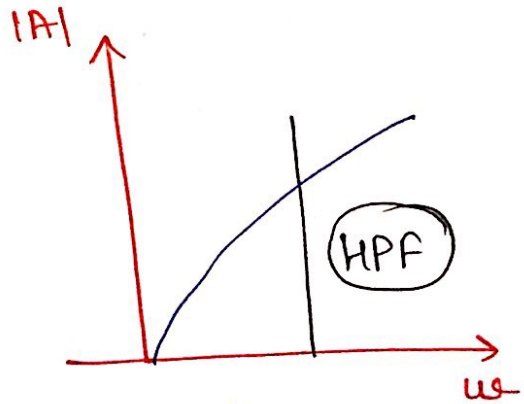
② **High Pass Filter:**



$$V_o = \left(\frac{V_{in}}{R+\frac{1}{j\omega C}}\right)R$$

$$\frac{V_o}{V_{in}} = \frac{R}{1+j\omega RC}\cdot j\omega C = \frac{1}{\frac{1}{j\omega RC}+1}$$

$$|A| = \frac{1}{\sqrt{1+\left(\frac{1}{\omega RC}\right)^2}}$$

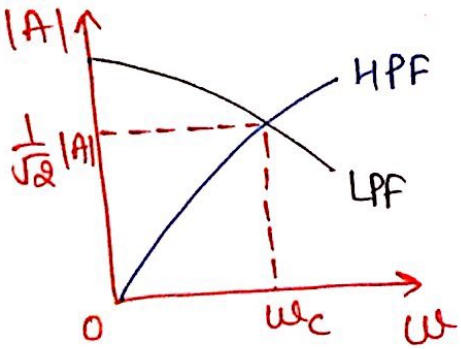


i.e gain is high at high ~~frequencies~~. Hence, called HPF. example: Differentiator CKT.

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Cut off Freq.

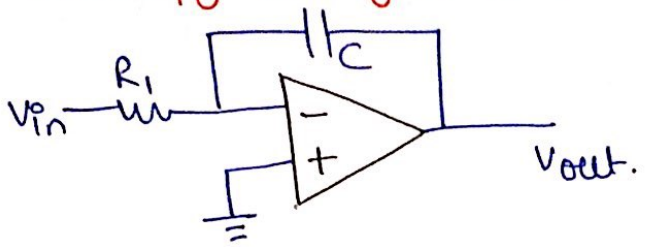
The frequency at which gain becomes $1/\sqrt{2}$ times of the maximum value.



$$\omega_c = \frac{1}{R_f C_f} \rightarrow \text{(LPF)}$$

$$\omega_c = \frac{1}{RC} \rightarrow \text{(HPF)}$$

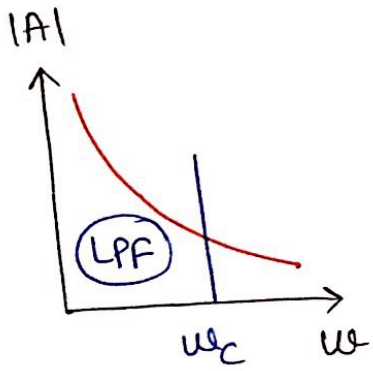
Que 1 Identify the type of filter:



Soln:-

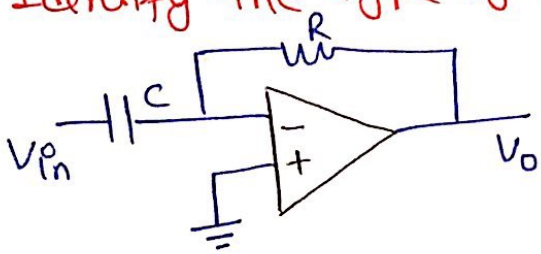
$$A = -\frac{R_f}{R_1} = -\frac{1}{j\omega R_1 C} = \frac{j}{\omega R_1 C}$$

$$|A| = \frac{1}{\sqrt{(\omega RC)^2}} = \frac{1}{\omega RC}$$



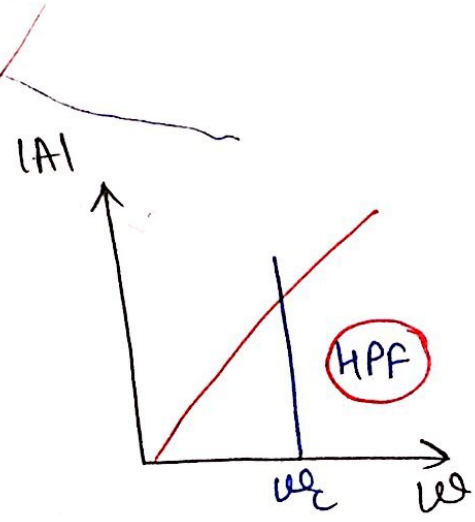
$$\omega_c = \frac{1}{R_1 C}$$

Que 2 Identify the type of filter:



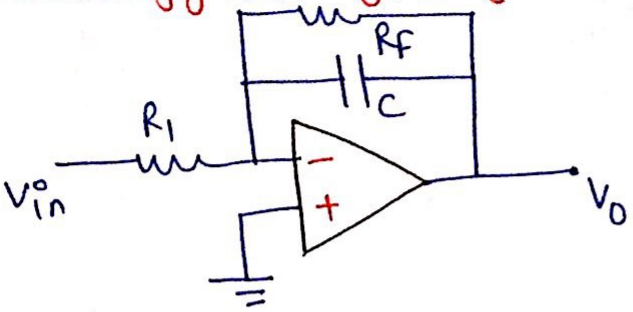
$$\frac{V_o}{V_{in}} = \frac{-R}{1/j\omega C} = -j\omega RC$$

$$|A| = \omega RC$$



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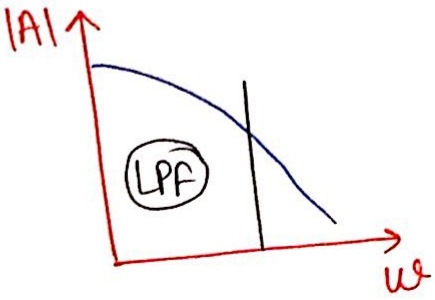
Que 3 Identify the type of filter:



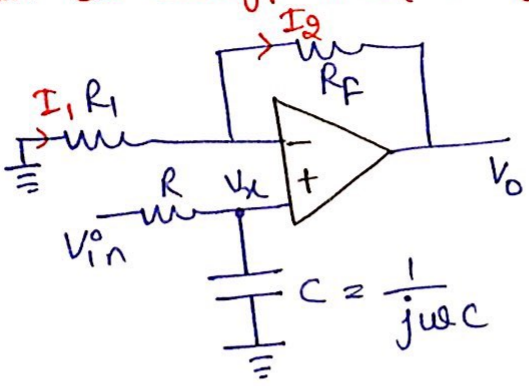
$$Z_f = \frac{R_f \cdot \frac{1}{j\omega C}}{R_f + \frac{1}{j\omega C}} = \frac{R_f}{1 + j\omega R_f C}$$

Soln:- $$\frac{V_o}{V_{in}} = -\frac{Z_f}{R_1} = -\frac{R_f}{R_1(1 + j\omega R_f C)}$$

$$|A| = \frac{R_f}{R_1\sqrt{1^2 + \omega^2 R_f^2 C^2}}$$



Que 4 Identify the type of filter and also determine gain at cutoff frequency?



$$V_x = \left(\frac{V_{in}}{R + \frac{1}{j\omega C}}\right)\frac{1}{j\omega C}$$

$$V_x = \frac{V_{in}}{1 + j\omega RC}$$

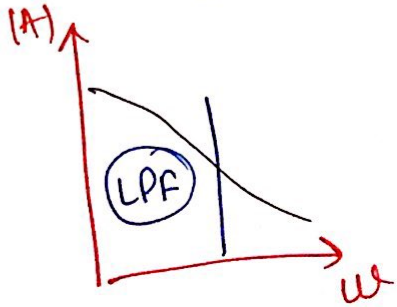
Soln:- $I_1 = I_2$

$$\frac{0 - V_x}{R_1} = \frac{V_x - V_o}{R_1} \Rightarrow V_o = \left(1 + \frac{R_f}{R_1}\right)\frac{V_{in}}{1 + j\omega RC}$$

$$\left|\frac{V_o}{V_{in}}\right| = \left(1 + \frac{R_f}{R_1}\right)\frac{1}{\sqrt{1 + \omega^2 R^2 C}}$$

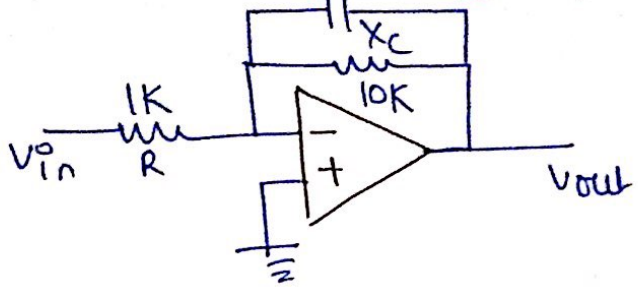
at $\omega = \omega_c = 1/RC$

$$\boxed{|A| = \frac{1}{\sqrt{2}}\left(1 + \frac{R_f}{R_1}\right)}$$



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Ques In the OP-AMP circuit shown in the figure:



$X_C = 0.01\,\mu F$

V_{in} is a sinusodial input signal of frequency 10 Hz and V_0 is the output signal. The magnitude & Phase shift of gain, respectively, are close to the values:

a) $5\sqrt{2}$ and $\pi/2$ b) $5\sqrt{2}$ and $-\pi/2$

c) 10 and zero d) 10 and π

Soln:- $$V_0 = \frac{-X_C R_f}{(X_C + R_f)} \cdot \frac{1}{R} V_{in}$$

$$\frac{V_0}{V_{in}} = \frac{-10K\,X_C}{1K\left(1+\frac{R_f}{X_C}\right)X_C} = \frac{-10}{1+R_f/X_C}$$

$$X_C = \frac{1}{j\omega R_1}$$

$$A = \frac{-10}{R_1(1+j\omega R_f C_f)} \qquad \omega = 2\pi f.$$

$$A = \frac{-10K}{1K\left(1+j2\times 3.14\times 0.01\times 10^{-6}\times 10\times 10^{3}\right)}$$

$$A = \frac{-10}{1+0.00628j} \simeq (-10) \quad \cancel{|A|}$$

$|A| = 10$

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Phase angle:

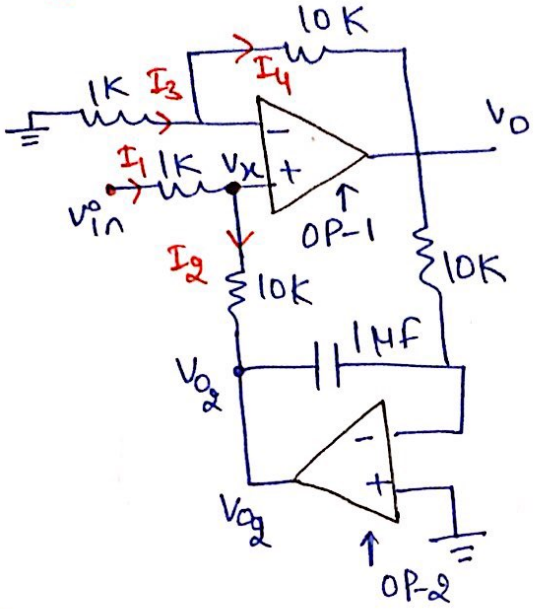
$$\angle A = \angle -10 - \angle 1 + j(0.00628)$$

$$\downarrow$$

$$180^\circ - \tan^{-1}\left(\frac{0.00628}{1}\right) \Rightarrow 180^\circ \text{ or } \pi$$

D

Que 6 A time varying signal v_{in} is fed to an OP-AMP circuit with output signal v_o as shown in the figure below. The circuit implements a:



a) HPF with $\omega_c = 16\pi$

b) HPF with $\omega_c = 100\pi$

c) HPF with $\omega_c = 100\pi$

d) LPF with $\omega_c = 16\pi$

Soln:-

For OP-AMP-1:

$$I_1 = I_2$$

$$\frac{V_{in} - V_x}{1K} = \frac{V_x - V_{o1}}{10K}$$

$$11V_x = V_{o1} + 10V_{in} \quad -(1)$$

$$I_3 = I_4$$

$$\frac{0 - V_x}{1K} = \frac{V_x - V_o}{10K} \Rightarrow V_o = 11V_x$$

$$V_o = V_{o1} + 10V_{in} \rightarrow \text{by } (1)$$

For OP-AMP: 2

$$\frac{V_{o1}}{V_o} = -\frac{R_f}{R_1}$$

$$V_{o1} = -\frac{V_o}{j\omega R_1 C} \quad -(2)$$

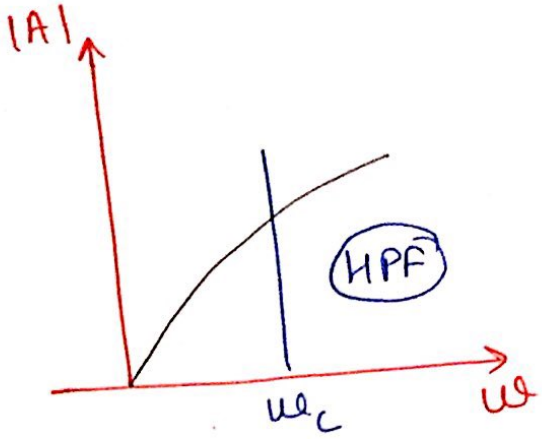
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$$V_o = 10V_{in} - \frac{V_o}{j\omega R_1 C} \quad \text{— by (2)}$$

$$V_o\left[1 + \frac{1}{j\omega R_1 C}\right] = 10V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{10}{1 + \frac{1}{j\omega R_1 C}}$$

$$|A| = \frac{10}{\sqrt{1 + \frac{1}{\omega^2 R_1^2 C^2}}}$$

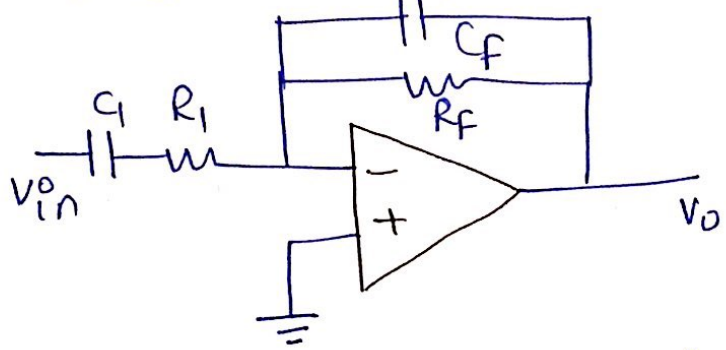


$$\omega_c = \frac{1}{R_1 C} = \frac{1}{10K \times 10\mu F} = 10^2 \text{ Rad/sec.}$$

$$f_c = \frac{\omega_c}{2\pi} = \frac{100}{2 \times 3.14} = 16\,Hz$$ [A]

③ **Band Pass Filter:**

a band pass filter pass signals only in a certain band of frequencies.



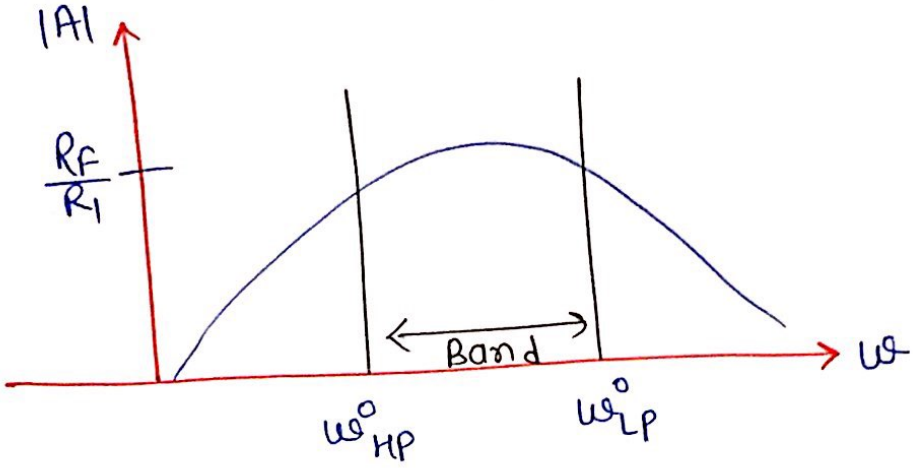
$$Z_{in} = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$

$$Z_f = R_f \cdot \frac{1}{j\omega C_f} \Big/ \left(R_f + \frac{1}{j\omega C_f}\right) = \frac{R_f}{1 + j\omega R_f C_f}$$

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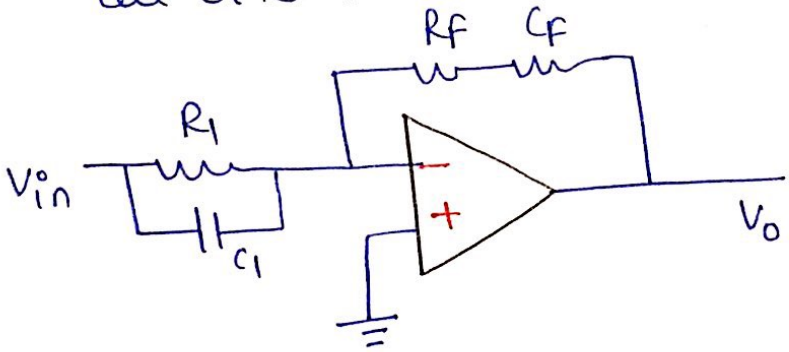
$$\frac{V_{out}}{V_{in}} = -\frac{Z_f}{Z_{in}} = -\frac{R_f}{R_1}\,\frac{1}{(1+j\omega R_f C_f)} \times \frac{1}{\left(1-\frac{j}{\omega R_1 C_1}\right)}$$

$$|A| = \frac{R_f}{R_1}\,\frac{1}{\sqrt{1+\omega^2 R_f^2 C_f^2}} \times \frac{1}{\sqrt{1+\frac{1}{\omega^2 R_1^2 C_1^2}}}$$



④ Band stop Filter:

It rejects a band of frequencies, while passing all others.

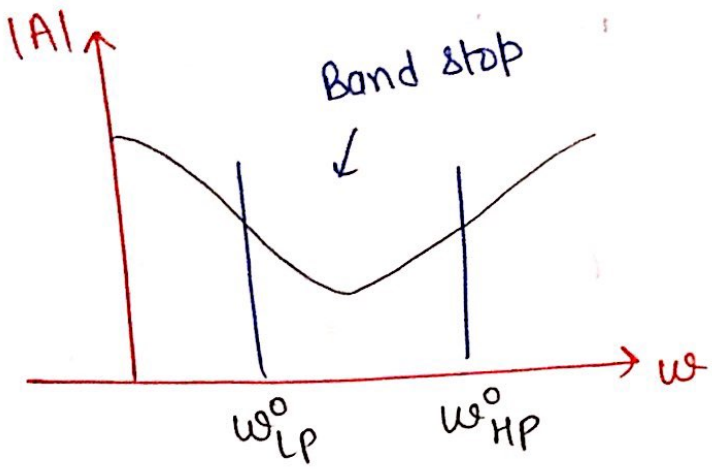


$$Z_f = \frac{1+j\omega R_f C_f}{j\omega R_f} \quad ; \quad Z_{in} = \frac{R_1}{1+j\omega R_1 C_1}$$

$$\frac{V_0}{V_{in}} = -\frac{R_f}{R_1}\left(1-\frac{j}{\omega R_f C_f}\right)(1+j\omega R_1 C_1)$$

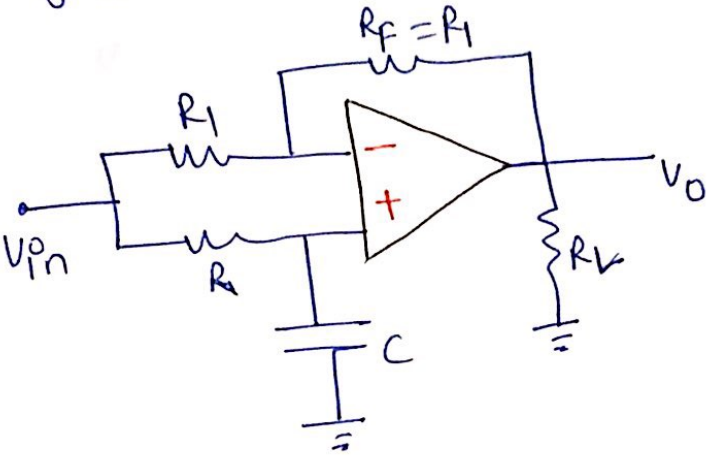
$$|A| = \frac{R_f}{R_1}\sqrt{\left(1+\frac{1}{\omega^2 R_f^2 C_f^2}\right)(1+\omega^2 R_1^2 C_1^2)}$$

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⑤ All Pass filter:

Passes all frequency components of input signal without attenuation.



$$\frac{V_{out}}{V_{in}} = \frac{1 - j\omega RC}{1 + j\omega RC} \qquad \omega = 2\pi f.$$

$$\phi = -2\tan^{-1}\left(\frac{2\pi f RC}{1}\right)$$

example: If R=15KΩ ; C=0.01μF, and freq. of i/p signal = 2KHz find phase shift?

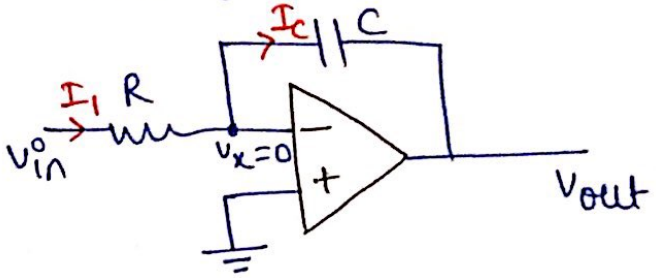
Soln:- $\phi = -2\tan^{-1}(2 \times 3.14 \times 2 \times 10^{3} \times 15 \times 10^{3} \times 0.01 \times 10^{-6})$

$$\phi = -124^{\circ}$$

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→ **Integrator:** (act as LPF)

Process of continuous addition



$$I = I_C$$

$$\frac{V_{in}-0}{R} = C\frac{dV_C}{dt}$$

$$V_C = 0 - V_0$$

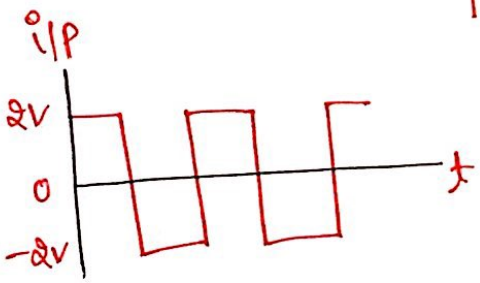
$$V_C = -V_0$$

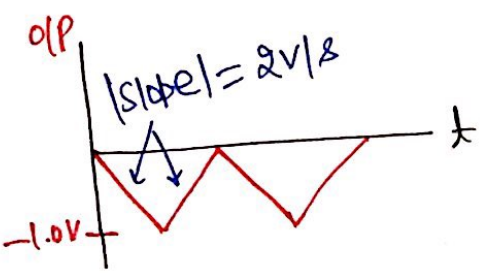
$$\frac{V_{in}}{R} = -C\frac{dV_0}{dt}$$

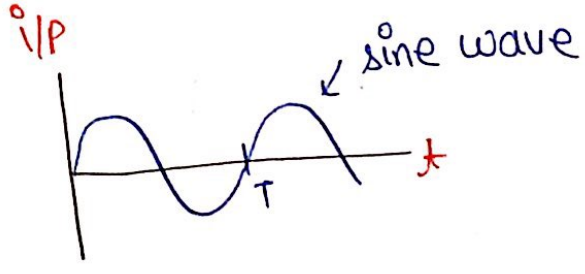
$$dV_0 = -\frac{1}{RC}V_{in}\,dt$$

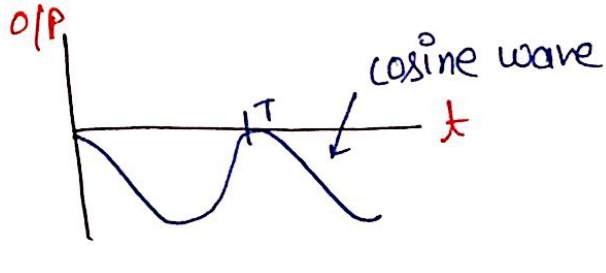
$$\boxed{V_0 = -\frac{1}{RC}\int_0^t V_{in}\,dt}$$

input	output
(square)	(triangular)
sine wave	cosine wave



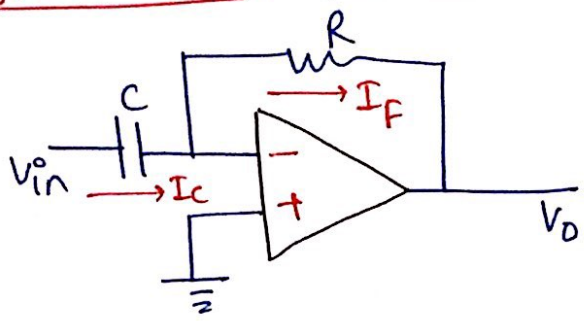






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→ Differentiator: (act as HPF)



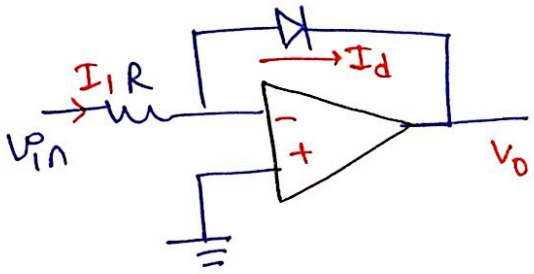
$$I_C = I_F$$

$$C\frac{dV_c}{dt} = \frac{0 - V_{out}}{R}$$

$$\boxed{V_{out} = -RC\frac{d}{dt}(V_{in})}$$

	input	output
①	square	spikes / Dirac Delta fxn
②	sine	cosine
③	triangular	square

→ Log amplifier:



$$I_1 = I_D$$

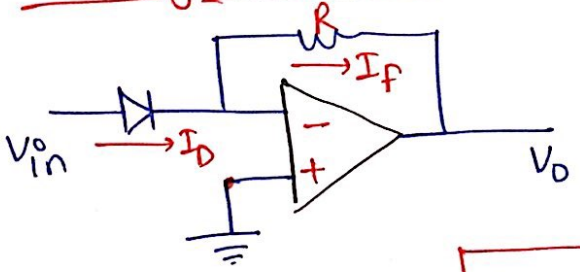
$$\frac{V_{in} - 0}{R} = I_0 e^{(-V_0)/\eta V_T}$$

$\rightarrow V_0 = -V_d$

$$\boxed{V_0 = -\eta V_T \log\left(\frac{V_{in}}{I_0 R}\right)}$$

$V_T = 25mV$ at $T = 300K$ (Threshold voltage)

→ Anti Log Amplifier:



$$I_D = I_F$$

$$I_0 e^{V_d/\eta V_T} = \frac{0 - V_{out}}{R}$$

$$\boxed{V_0 = -I_0 R\, e^{V_{in}/\eta V_T}}$$

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*** Feedback:

Series: voltage change but current doesn't change

Parallel: voltage same but current change

Input: variable Output: constant

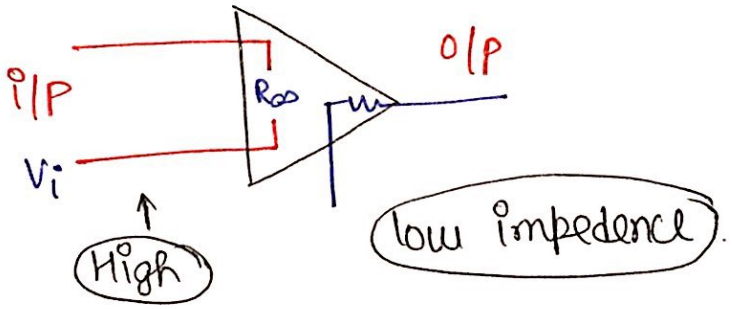
1) Series - Series (input: VC, output: CS)

2) Series - Shunt (Parallel) (input: VC, output: VS)

3) Shunt - Series (input: CC, output: CS)

4) Shunt - Shunt (input: CC, output: VS)

*** OP-AMP converts High input impedence into low output impedence.



*** OP-AMP with finite gain:

1) For inverting OP-AMP

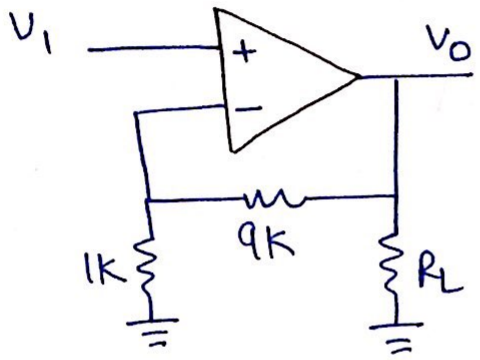
$$V_o = \frac{-R_f/R_1}{1 + \frac{(R_f/R_1)}{A_{open}}}$$

2) For non-inverting OP-AMP

$$V_o = \frac{1 + R_f/R_1}{1 + \frac{(1 + R_f/R_1)}{A_{open}}}$$

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Que! Find closed loop gain & configuration of given circuit if open loop gain is 10^5



a) series-shunt, $A_f = 9$
b) series-series, $A_f = 10$
c) series-shunt, $A_f = 10$
d) shunt-shunt, $A_f = 10$

Sol^n:- input voltage changes: series
o/p voltage fixed: shunt

$$A_f = \frac{(1+R_f/R_1)}{1+\frac{(1+R_f/R_1)}{A_{open}}} = \frac{1+9/1}{1+\frac{(10)}{10^5}}$$

$$= \frac{10}{1+10^{-4}} \simeq 10$$

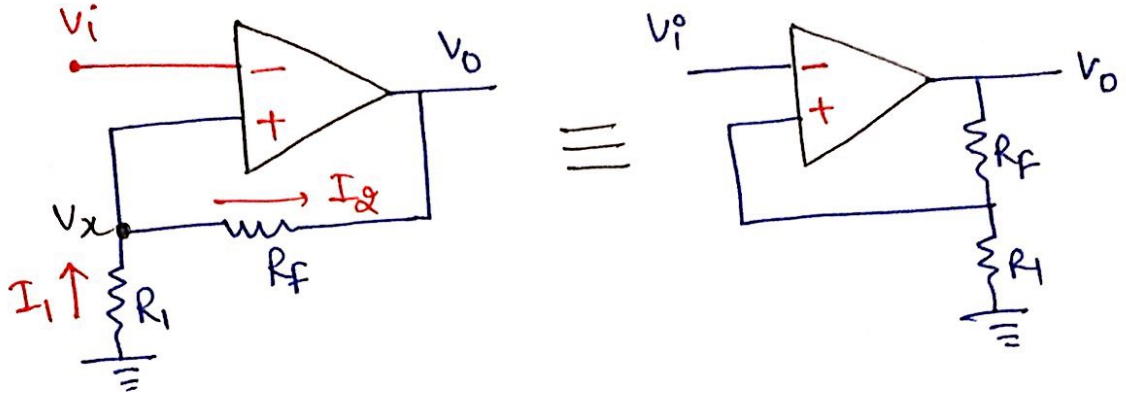
C

POSITIVE FEEDBACK OP-AMP

→ OP-AMP Here, behaves as waveform generator (basically a square wave)

→ also called as regenerative comparator.

→ Basic CKT used for the feedback condition is called as schmit trigger.



→ in the +ve feedback condition:

output range: $+V_{sat}$ to $-V_{sat}$.

now, $I_1 = I_f$

$$\frac{0 - V_x}{R_1} = \frac{V_x - V_o}{R_f}$$

$$\Rightarrow V_x = \left(\frac{R_1}{R_1 + R_f}\right) V_o$$

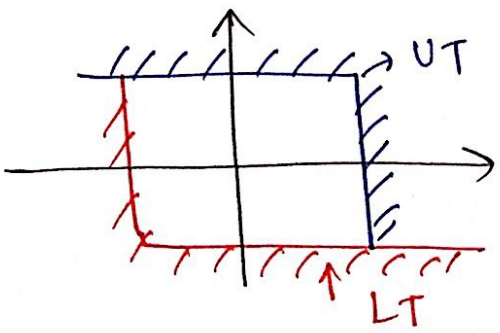
feed back factor

$$V_x = \left(\frac{R_1}{R_1 + R_f}\right) V_o$$

$+V_{sat}$ $\quad$ $-V_{sat}$

$$V_{UT} = V_{sat} \times \frac{R_1}{R_1 + R_f}$$

$$V_{LT} = -V_{sat} \times \frac{R_1}{R_1 + R_f}$$

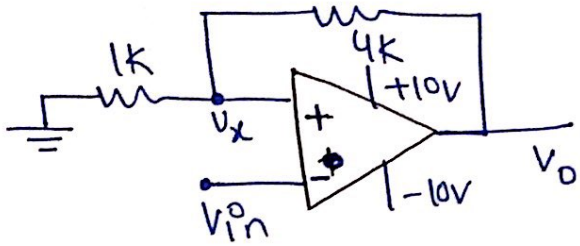


Hysteresis curve = $V_{UT} - (-V_{LT})$

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example: Determine the Hysteresis voltage for the following circuit:

①



Soln:- $V_x = \left(\frac{1}{1+4}\right) V_o = V_{in}$

$V_o = 5 V_{in}$

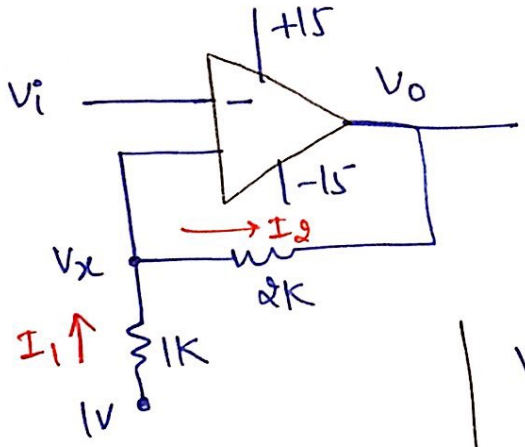
$V_{UT} = \frac{1}{5} \times 10 = 2V$

$V_{LT} = -\frac{1}{5} \times 10 = -2V$

Hysteresis voltage $= 2V - (-2V)$

$= 4V$

②



Soln:- $I_1 = I_2$

$\frac{2 - V_x}{1K} = \frac{1 - V_o}{2K}$

$3V_x = V_o + 2$

$V_x = \frac{V_o + 2}{3}$

$V_{UT} = \frac{15+2}{3} = \frac{17}{3}$

$V_{LT} = \frac{-15+2}{3} = \frac{-13}{3}$

$H = V_{UT} - V_{LT}$

$H = 10V$

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→ **Oscillator**: (+ve feedback)

in oscillator, +ve feedback is used.

Oscillator's gain = $\frac{A}{1-A\beta}$ $\frac{A}{1+A\beta}$ → OP-AMP gain (amplification)

sinusodial cond^n: $A\beta = 1$ Barkhausen criteria

1) **Low frequency Oscillator** (audio Frequency)

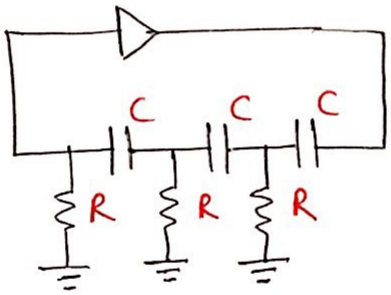
a) **R-C Phase shift oscillator**:

in CE = 180° Phase shift

↑ Preffered because its current gain & voltage gain are HIGH

→ minimum 3RC stage are required to Produce a Phase shift of 180°.

Example: The oscillator CKT shown in figure has an ideal inverting amplifier. Its frequency of oscillation (in Hz) is:

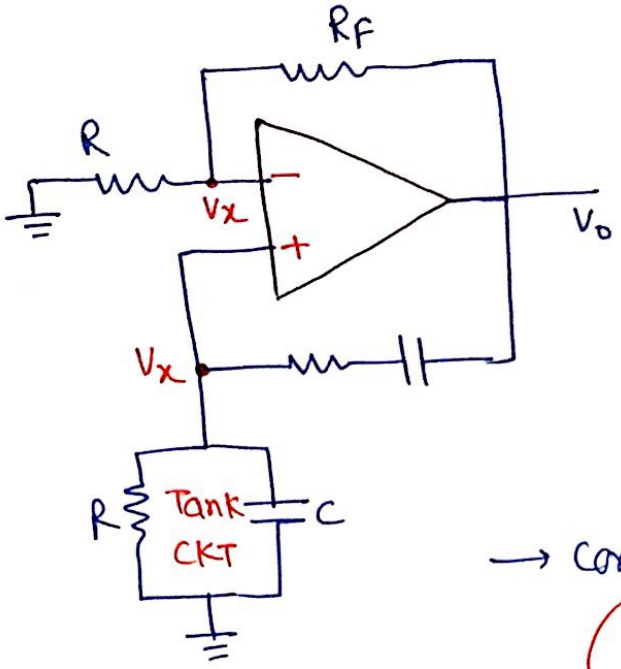


Soln. $f_{BJT} = \frac{1}{2\pi RC\sqrt{6+\frac{R_C}{R}}}$ $R_C = 0$

$f_{OP\text{-}AMP} = \frac{1}{2\pi RC\sqrt{6+0}} = \frac{1}{2\pi\sqrt{6}RC}$

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b) weins Bridge oscillator:



→ works in non-inverting mode

→ no additional Phase shift is required

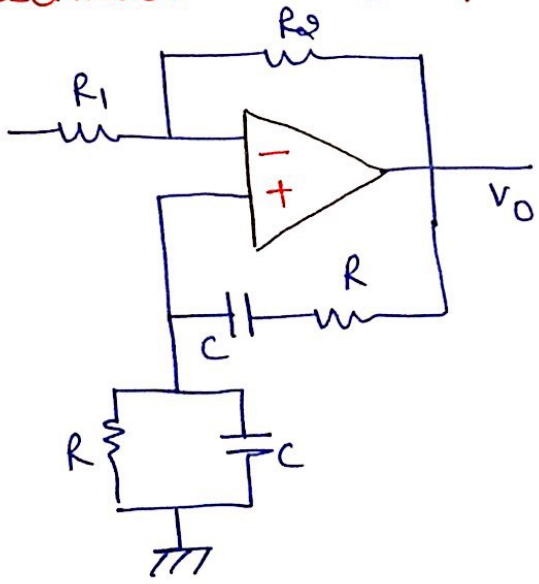
→ cut off frequency

$$f_0 = \frac{1}{2\pi RC}$$

→ cond^n to see peak:

$$\frac{1}{3}\left(1+\frac{R_f}{R_1}\right) \geq 1$$

example: what should be the values of the components R & R_2 such that the frequency of wein bridge oscillator is 300 Hz?



[Given: C = 0.01 μF & R_1 = 12K]

a) R = 48KΩ & R_2 = 12KΩ

b) R = 26KΩ & R_2 = 24KΩ

c) R = 530KΩ & R_2 = 1MΩ

d) R = 53KΩ & R_2 = 24KΩ

Soln:- $f_0 = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_0 C}$

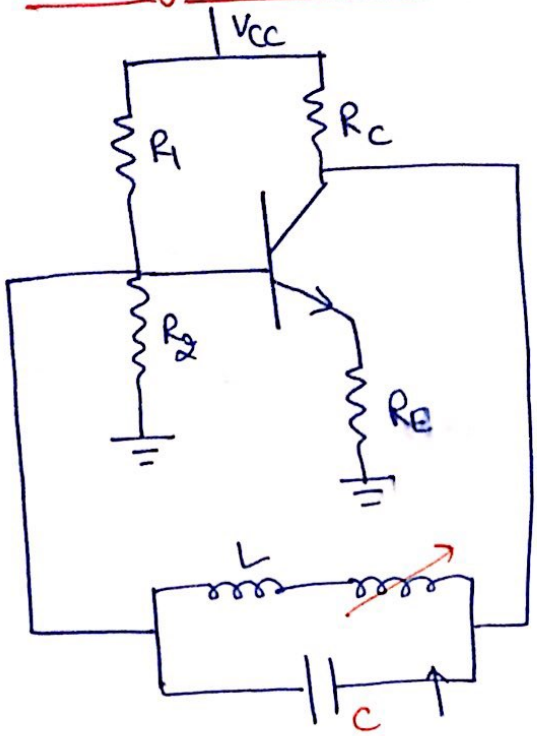
$$R = \frac{1}{2 \times 3.14 \times 300 \times 0.01 \times 10^{-6}} = 53K$$ **D**

cond^n: $1+\frac{R_f}{R_1} \geq 3 \Rightarrow \frac{R_f}{R_1} \geq 2 \Rightarrow R_2 = 24K\Omega$

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2> High Frequency Oscillator:

a> Heartly Oscillator:



$$\omega = \frac{1}{\sqrt{LC}}$$

$$= \frac{1}{\sqrt{L_{eq} C_{eq}}}$$

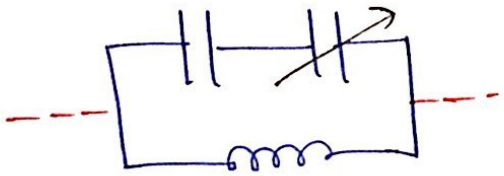
$$\omega = \frac{1}{\sqrt{(L_1+L_2)C}} \geq 1$$

$$f = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

Phase shift = 180°

b> Colpits Oscillator:

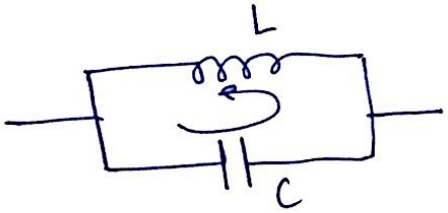
Same as Hartly oscillator except tank circuit.



$$\omega = \sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)}$$

Note: Tank circuit



$\omega = 0$ (dc) $\omega \neq 0$ (ac)

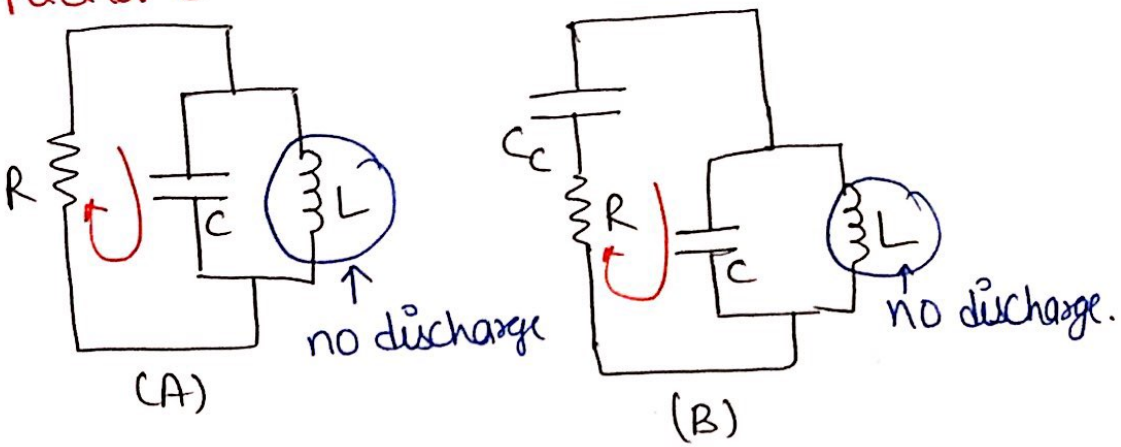
$\tau = RC$



L → only oscillation no discharge

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Qu 3 Two LCR circuit A & B are shown, where $C_c << C$ at $t=0$, a charge Q is put on the capacitor C



in which CKT charge will decay faster?

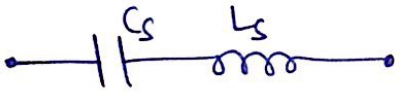
Soln:- $\tau = R \times C$

in fig.(A): $\tau = 0$ no time required

in fig (B): $\tau = R \times C_c$ some time required.

Fig (A)

→ **CRYSTAL OSCILLATOR:**



$$f = \frac{1}{2\pi\sqrt{L_s C_s}}$$

↑ Resonant Frequency

→ **Quadrature Oscillator:**

generates 2 signals that are in quadrature, i.e out of phase by 90°.

→ requires 2 OP-Amps and 3 RC CKT.

$$f_0 = \frac{1}{2\pi RC}$$

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ADC & DAC

→ Characteristic Parameter of DAC:

DAC: Digital to analog convertor

1) **Resolution / Precession**: change in analog value, due to 1-bit increment at LSB.

$$\text{Resolution} = \frac{V_r}{2^n - 1}$$

$n \rightarrow$ no. of bits.

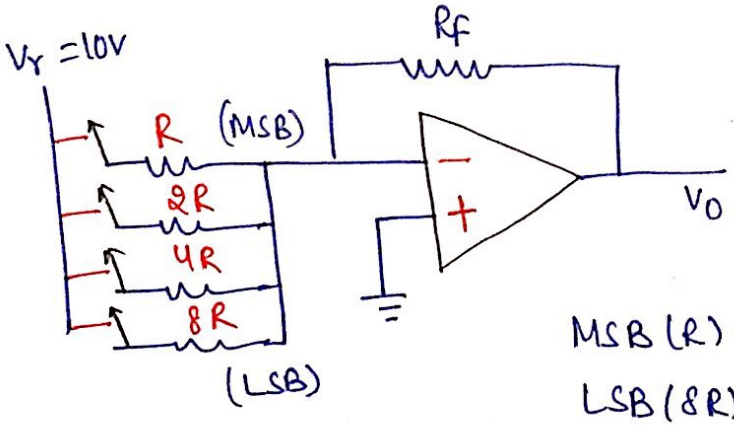
2) **Percentage Resolution**:

$$\%R = \frac{1}{2^n - 1} \times 100\%$$

3) Full scale voltage: $V_F = V_r$

4) Analog voltage: $V_a = \text{Resolution} \times \text{Decimal eq.}$

→ 1) Weighted Resistor type DAC:



MSB (R) → more current

LSB (8R) → less current.

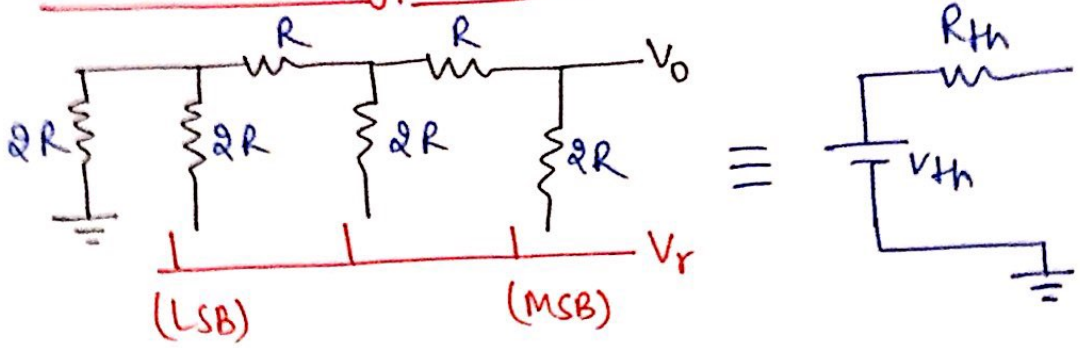
example: Binary = 1010 & V_r = 10V ; R = 1K

LSB current = 0A

MSB current = $\frac{10V - 0V}{1K}$ = 10mA.

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→ 2) R-2R ladder type DAC:

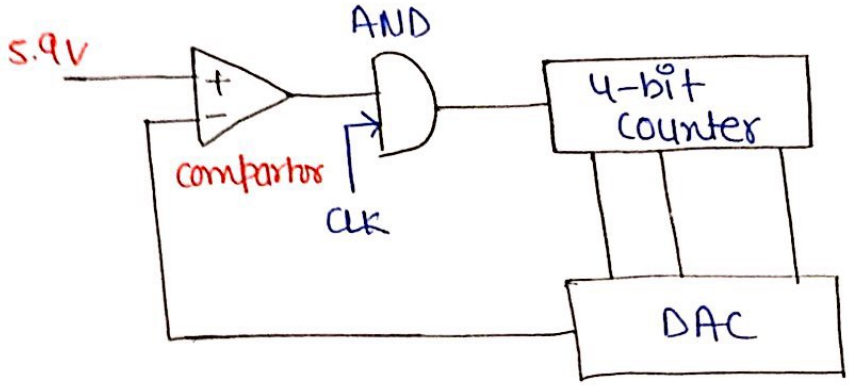


V_{analog} = Resolution × Decimal equivalent.

$$V_a = \frac{V_r}{2^n} \times \text{Dec. eq.}$$

Analog to Digital convertor:

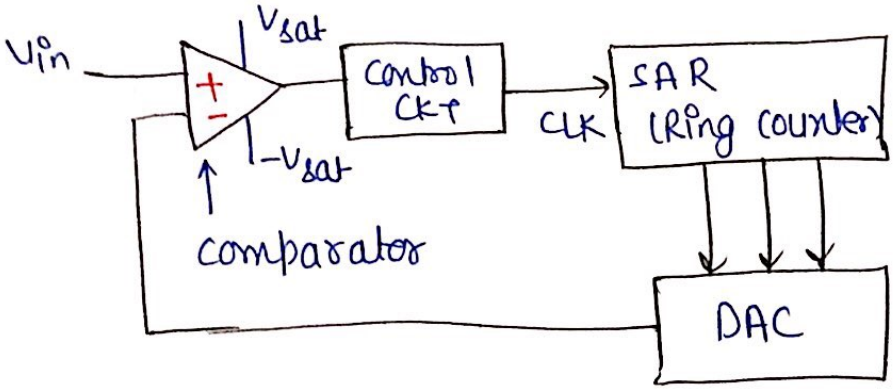
→ Counter type ADC:



max. no. of clocks = $2^n - 1$

*** max. conversion time = $(2^n - 1) \times T_{CLK}$

→ Successive Approximation Registor type convertor:



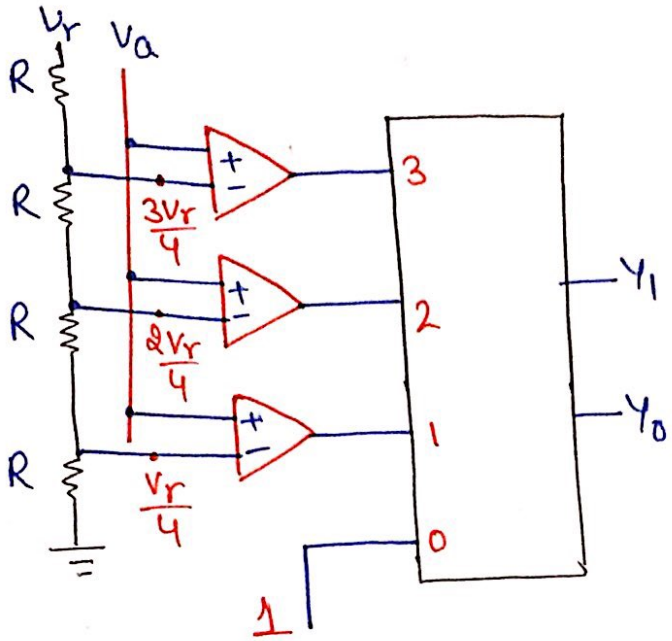
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conversion time $\propto$ n (f-f)

$\propto$ analog input.

*** maximum conversion time = $n \times T_{clk}$

→ Flash type ADC:



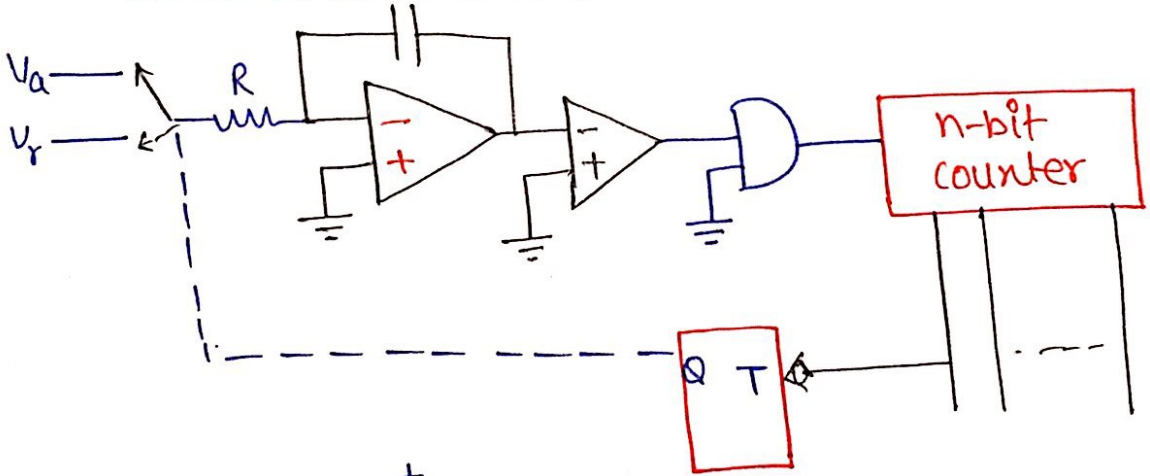
→ no. of Resistors: 2^n

→ no. of comparator: $2^n - 1$

→ max conversion time = T_{CLK}

→ Fast ADC

→ Dual slope Integrator:

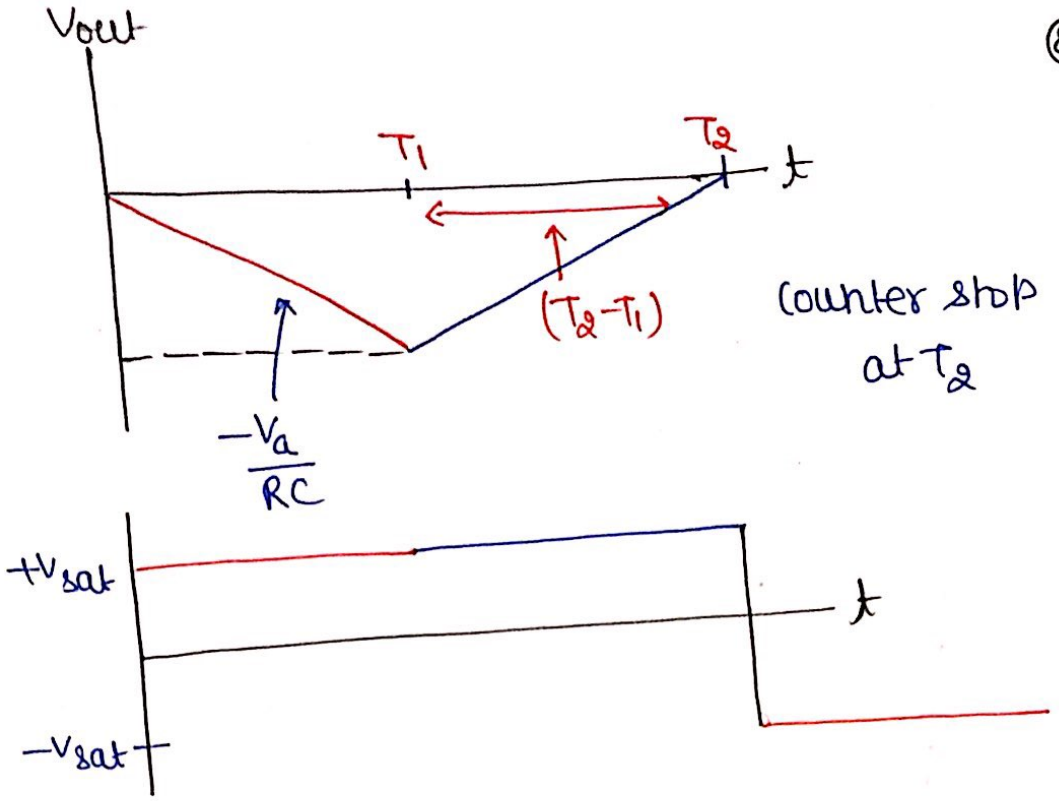


$$V_0 = -\frac{1}{RC}\int_0^t V_a\,dt \rightarrow \text{integrator}$$

$V_0 = -\frac{1}{RC} V_a \cdot t$

$y \quad m \quad x$

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$$T_1 = 2^n \times T_{CLK}$$

$$V_{out} = \frac{V_r}{RC}(t - T_1) - \frac{V_a}{RC} T_1$$

$$T_2 - T_1 = (2^n - 1) \times T_{CLK}$$

Que! The conversion time of an 8-bit successive approximation counter with 1MHz clock is nearly:

a) 8 μsec b) 128 μsec c) 256 μsec d) 512 μsec

Sol^n:- Conversion time of succesive approx counter

$$= n \times T_{CLK}$$

$$= n \times \frac{1}{f_{CLK}} = \frac{8}{1 \times 10^{-6}}$$

$$= 8 \text{ μsec}$$ [A]

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Data linked Question:

A dual slope ADC uses a 16-bit counter with a 5MHz, clock. If maximum input voltage is +12 volts and maximum integrator output for maximum count is −10 volts. If resistor used in integrator is 100KΩ then

Que 2 what is conversion period of dual slope ADC:

a) 5ms b) 10ms c) 13ms d) 26ms

Soln:- $T_2 - T_1 = (2^n - 1) \times T_{clk}$

$= ((2)^{16} - 1) \times \frac{1}{f_{clk}} = \frac{65,535}{5 \times 10^6}$

$= \frac{13107}{10^6} = 13ms$

C

Que 3 what is the value of capacitor used:

a) 0.48 μF b) 1 μF c) 0.16 μF d) 0.32 μF

Soln:- $V_0 = \frac{-V_a T}{RC} = -10$

$C = \frac{V_a T}{10 \times R} = \frac{12 \times 13 \times 10^{-3}}{10 \times 100 \times 10^3}$

$= 0.16 \mu F$

C

Que 4 The largest analog output voltage from a 6-bit DAC which produces 1.0 V output for a digital for a digital input of 010100, is:

a) 1.6V b) 2.9V c) 3.15V d) 5.0V

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Soln:- 01|01|00 ⇒ Decimal eq. = 16+4 ⇒ 20

analog voltage = Resolution x Decimal eq.

$$1V = \frac{V_r}{2^n - 1} \times 20 \Rightarrow \frac{V_r}{(2^6 - 1)} \times 20$$

$$V_r = \frac{63}{20} = 3.15\,V$$

C

Ques what should be the clock frequency of a 6-bit A/D converter so that maximum conversion time is 32 μs?

a) 1MHz b) 2MHz c) 0.5MHz d) 4MHz

Soln:- max. conversion time = $(2^n - 1) \times T_{CLK}$

$$32\,\mu s = (2^6 - 1)\,T_{CLK}$$

$$\frac{1}{T_{CLK}} = \frac{63}{32 \times 10^{-6}}$$

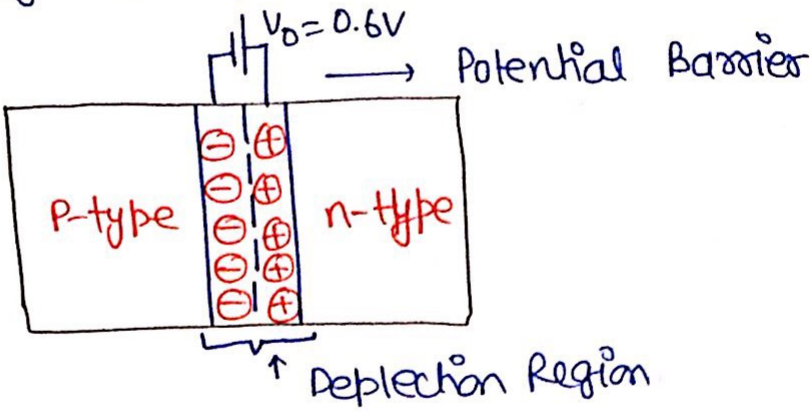
$$f_{CLK} = 2\,MHz$$

B

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JUNCTION THEORY

→ **P-N Diode:** In an intrinsic semiconductor, from 1 side p-type substance and from another side n-type substance are diffused. The point at which they meet form a P-N diode.



Width of Depletion Region:

$$\text{width}(w) = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_d} + \frac{1}{N_a}\right](V_0 + V_{RB})}$$

where, N_d & N_a are doping concentrations

q = charge ; $\varepsilon = \varepsilon_0 \varepsilon_r$

$w \simeq 0.5\,\mu m$.

Que! Determine the width of Depletion Region of P-N junction whose $N_d = 10^{16}$ atoms/cm^3, $\varepsilon_r = 11.67$, $V_{RB} = 0$, $V_0 = 0.6$.

Soln.

$$w = \sqrt{\frac{2 \times 8.85 \times 10^{-14}}{1.6 \times 10^{-19} C}\left(\frac{1}{10^{16}}\right)(0 + 0.6)}$$

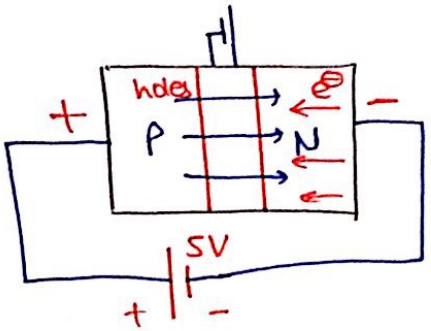
$$= \sqrt{7.746}\ \mu m$$

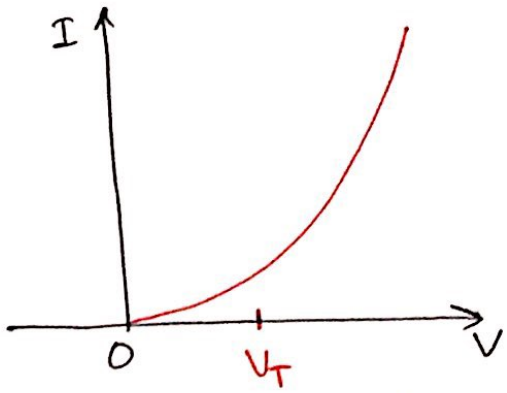
$$= 2.78\ \mu m.$$

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Biasing of P-N junction:

1) Forward Biasing: used to decrease the width of depletion Region.





Steady state: capacitance effect developed called Diffusion capacitance.

life time (τ) = RC_D

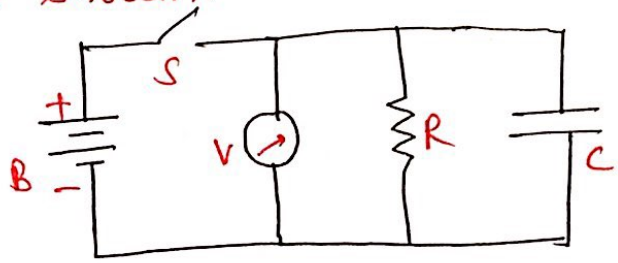
*** Diffusion capacitance decreases with temp.

$$C_D = \frac{\tau}{R} = \frac{\tau}{\frac{\eta V_T}{I_D}} = \frac{\tau \left(I_0 e^{V_D/\eta V_T}\right)}{\eta V_T}$$

↑ decreases with temp.

↓ no effect.

Qu: The insulation resistance R of an insulated cable is measured by connecting it in parallel with a capacitor C, a voltmeter, and battery B as shown.



The voltage across the cable dropped from 150 V to 15V, 1000 seconds after the switch is closed. If the capacitance of cable is 5μF then

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its insulation resistance is approximately:

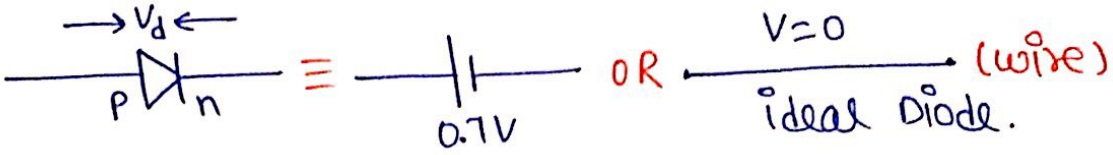
a) $10^9\Omega$ b) $10^8\Omega$ c) $10^7\Omega$ d) $10^6\Omega$

Soln:- $\tau = RC$

$$R = \frac{\tau}{C} = \frac{1000}{5\times10^{-6}} = 2\times10^8\ \Omega$$

$$R \approx 10^8\Omega$$ **B**

current through Diode:



$$I_d = I_0\left(e^{V_d/\eta V_T} - 1\right)$$ $I_0 \rightarrow$ leakage current

$$I_d \approx I_0\, e^{V_d/\eta V_T}$$

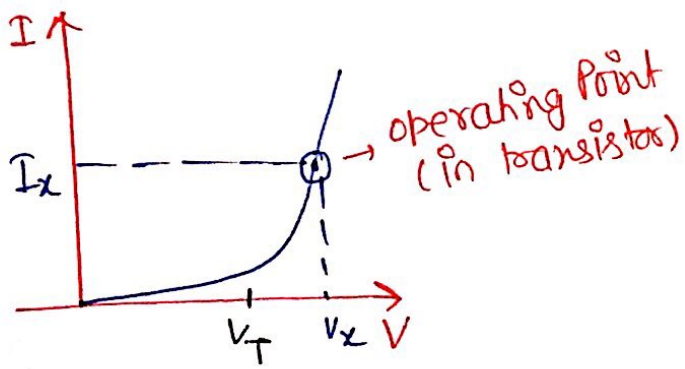
V_T = threshold voltage = $\frac{T}{1600}$

$V_T = 25$ mV at $T = 300$K

$I_d \propto$ temperature

*** → Foward Biased current (majority carrier current) is independent of temperature.

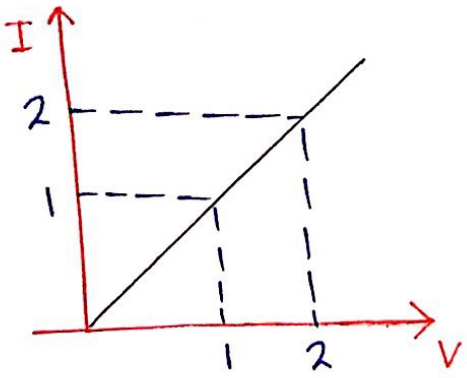
Static (D.C) Resistance:



$$R_x = \frac{V_x}{I_x}$$

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Dynamic Resistance (AC):



$$\frac{dy}{dx} = \frac{y_2 - y_1}{x_2 - x_1}$$

$$= \frac{2-1}{2-1} = 1$$

But for p-n diode, curve is not linear.

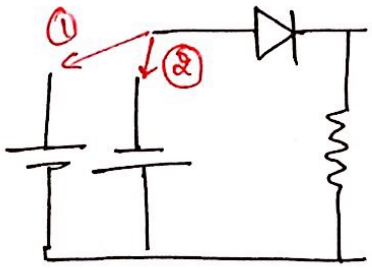
ac Resistance ≠ dc Resistance

$$R_{ac} = \frac{dV}{dI} = \frac{1}{(dI_D/dV_D)} \quad \& \quad I_D = I_0 e^{V_d/\eta V_T}$$

$$\boxed{R_{ac} = \frac{\eta V_T}{I_D}}$$

*** → Dynamic resistance increases with temp.

Que 3 Determine the current I across p-n junction diode, initially the position of switch was at ① for a long time and at that time current was 100 mA. Suddenly the position of switch was changed at ②. Determine the current at the time when the position was changed to ②.



a) 100 mA b) −100 mA

c) 0 mA d) none

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Soln:- at Position ①, saturation formed.

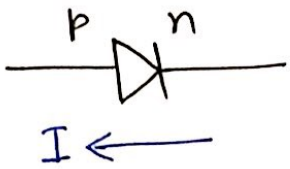


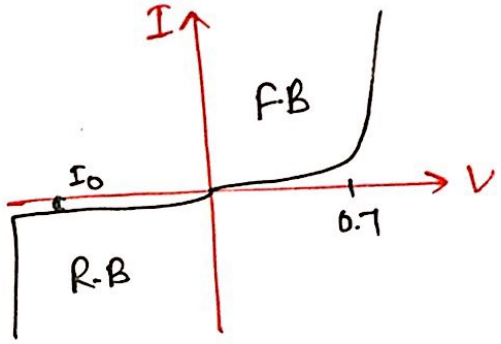
suddenly change to ②

$I = 100mA$ → for a small time

but for long time: $I = 0$

2) Reverse Biasing: used to increase the strength of contact potential i.e (width ↑es)





Transition capacitance:

Under R.B condition the capacitance effect developed is due to sudden transition of charge carriers.

transition charge ≡ Delta fxn (unit step) ≡ indeterminant

$$C_T = \frac{\varepsilon A}{w} \Rightarrow C_T = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_d}+\frac{1}{N_a}\right)(V_0+V_{RB})}}$$

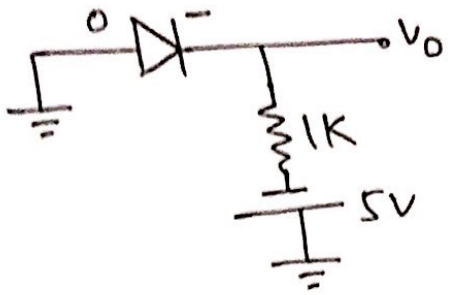
$$C_T = \frac{C_0}{\sqrt{1+\frac{V_{RB}}{V_0}}}$$ (C_0 → Junction capacitance)

$$\Rightarrow C_0 = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_d}+\frac{1}{N_a}\right)V_0}}$$

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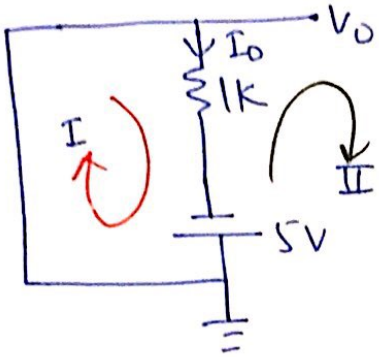
Examples:

① Determine the current I and output voltage V_o:



Soln:





apply loop I:

$I_o \times 1K - 5V = 0$

$I_o = \frac{5}{1K} = 5mA$

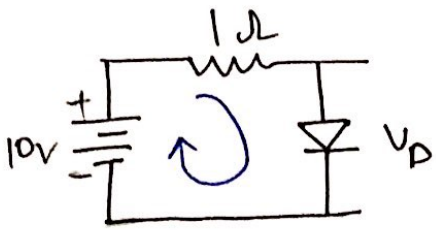
apply loop II: $I_o \times 1K - 5V + V_o = 0$

$(5mA \times 1K) - 5V = V_o$

$V_o = 0$

② A diode D shown in the circuit as an I-V relation which can be approx:

$$I_D = \begin{cases} V_D^2 + 2V_D & \text{for } V_D > 0 \\ 0 & V_D \leq 0 \end{cases}$$



The value of V_D in CKT is:

a) $(-1+\sqrt{11})V$ b) 5V

c) 8V d) 2V

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Soln 8- $-10V + I_D \times 1\Omega + V_D = 0$

$-10V + (V_D^2 + 2V_d) + V_D = 0$

$V_D^2 + 3V_D - 10 = 0$

$V_D^2 + 5V_D - 2V_D - 10 = 0$

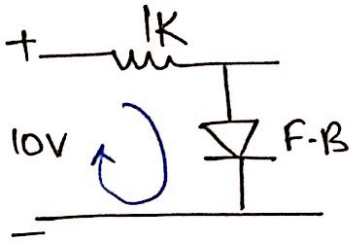
$V_D(V_D+5) - 2(V_D+5) = 0$

$(V_D+5)(V_D-2) = 0$

$V_D = -5V, 2V$

D

③ The I-V characteristic of the diode in the circuit below is given by



$$I = \begin{cases} (V_D - 0.7)/500 & \text{for } V \geq 0.7 \\ 0 & \text{for } V < 0.7 \end{cases}$$

where V is measured in volts and I is measured in amperes. The current I in the CKT is:

a) 10 mA b) 9.3 mA c) 6.2 mA d) 6.7 mA

Soln $-10V + I \times 1K + V_D = 0$

$-10V + \left(\frac{V_D - 0.7}{500}\right) \times 1000 + V_D = 0$

$-10V + 2V_D - 1.4 + V_D = 0$

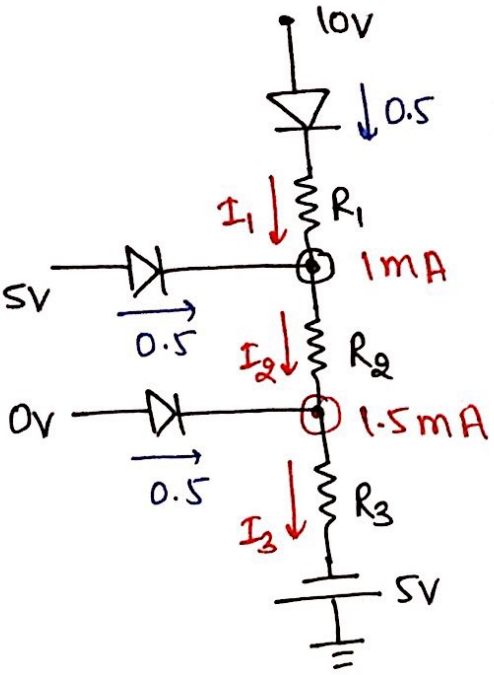
$3V_D = 11.4 \Rightarrow V_D = 3.8$ volts

$I = \left(\frac{3.8 - 0.7}{500}\right) \times 1000$ mA $= 6.2$ mA

C

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(4) Determine values of R_1, R_2 and R_3.



Assume that each diode is under F.B condition and supports a current of 0.5 mA.

Soln$^{n}_{o}$- $I_1 = 0.5\,mA$

$I_2 = 1.0\,mA$

$I_3 = 1.5\,mA$

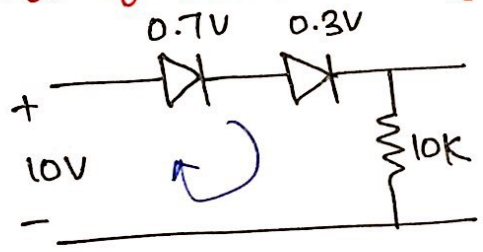
$$I = \frac{V_a - V_b}{R} \Rightarrow R = \frac{V_a - V_b}{I_1}$$

$$R_1 = \frac{10V - 5V}{0.5} = 10k\Omega$$

$$R_2 = \frac{5-0}{1} = 5k\Omega$$

$$R_3 = \frac{0-(-5)}{1.5} = 3.33k\Omega$$

(5) Determine output voltage (V_o) and output current (I_o) of the following circuit:



Soln$^{n}_{o}$- $-10V + 0.7V + 0.3V + V_o = 0$

$$V_o = 9V$$

$$I_o = \frac{V_o}{R_o} = \frac{9V}{10k} \Rightarrow I_o = 0.9\,mA$$

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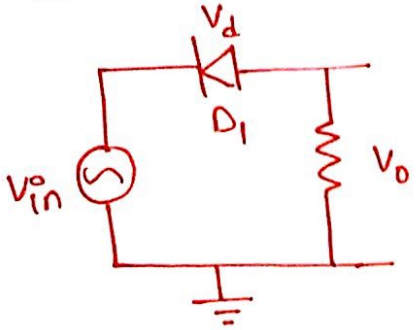
→ **CLLIPERS:**

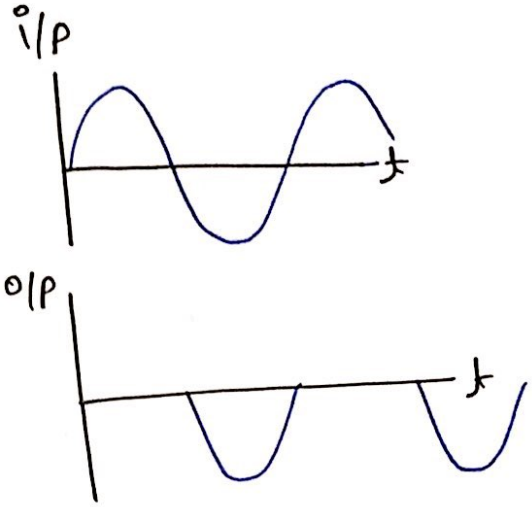
used to cut certain portion (either +ve or -ve) of the waveform.

Basic CKT elements: Resistor and Diode

1) Series clipper:

a) Series +ve clipper:





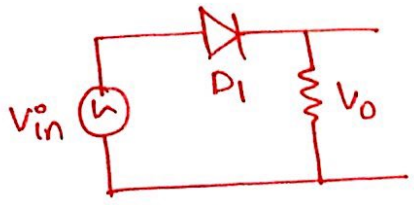
→ During +ve half cycle:

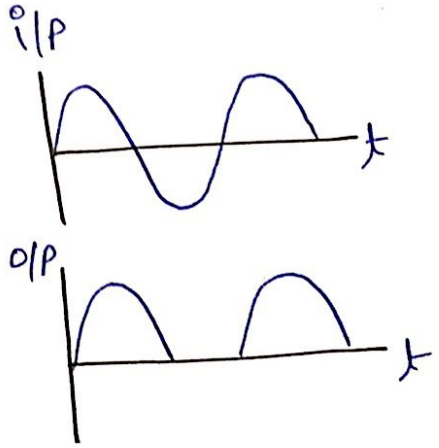
D_1 is R.B $\Rightarrow V_o = 0$

→ During -ve half cycle, D_1 is F.B

$V_o = V_{in} + V_d$

b) Series -ve clipper:





→ During +ve half cycle:

D_1 = F.B

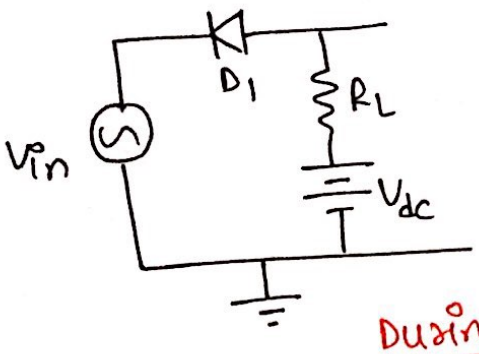
$V_o = V_d + V_{in}$

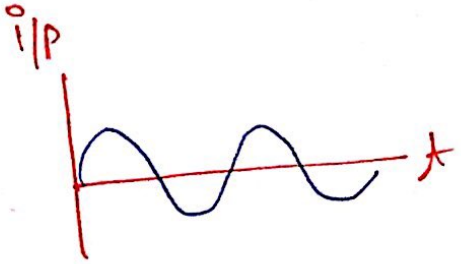
→ During -ve half cycle: D_1 = R.B $\Rightarrow V_o = 0$

*** its o/p is similar to Half wave Rectifier.

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Ques! Draw the output waveform for the given CKT:





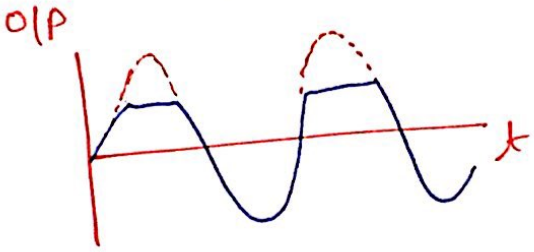
Soln:- During +ve half cycle

when $V_{in} < V_d + V_{dc} \Rightarrow V_o = V_{in} + V_d$

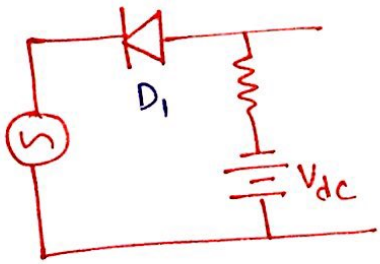
$V_{in} > V_d + V_{dc} \Rightarrow V_o = 0$

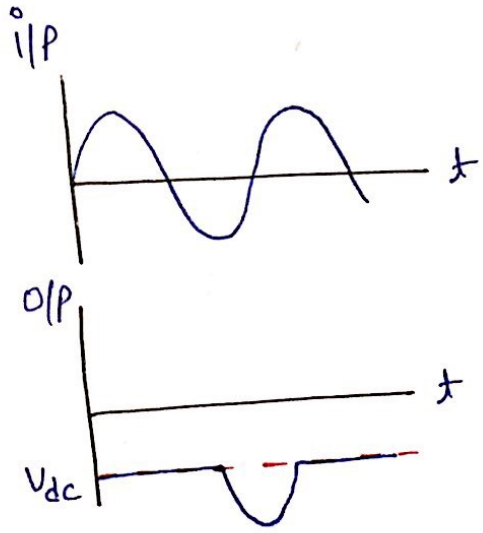
During -ve Half cycle: D_1 = F.B (always)

$V_o = V_{in} + V_d$



Ques 2





Soln:- During +ve Half cycle:

D_1 = R.B

$V_o = 0$

During -ve Half cycle:

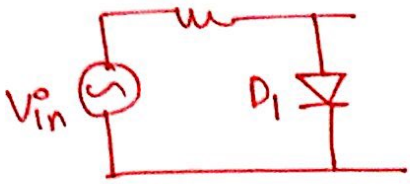
$V_{in} < V_d + V_{dc} \Rightarrow V_o = -V_{dc}$

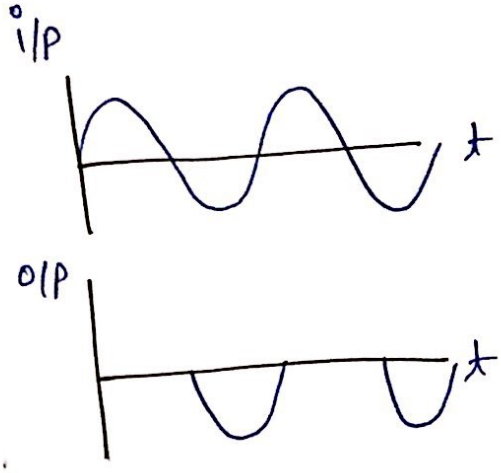
$V_{in} > V_d + V_{ds} \Rightarrow V_o = (V_{in} + V_{dc})$

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2) Shunt clippers:

a) Shunt +ve clipper:





During +ve Half cycle:

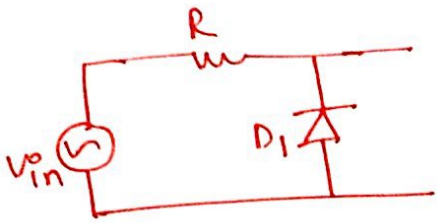
D_1 = F.B

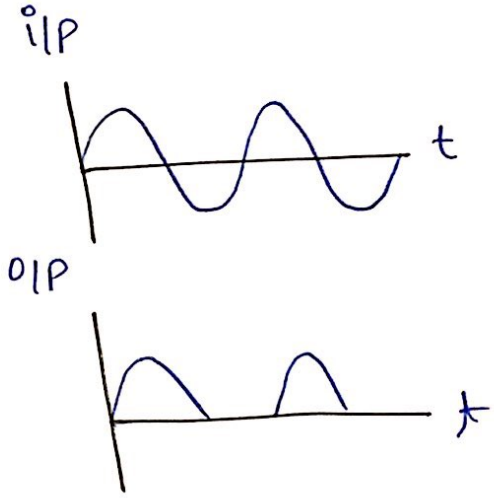
$V_o = V_d = 0$ for ideal diode.

During -ve Half cycle

$V_o = V_{in}$ volts.

b) Shunt -ve clipper:





During +ve Half cycle:

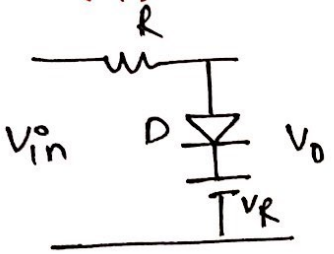
D_1 = R.B

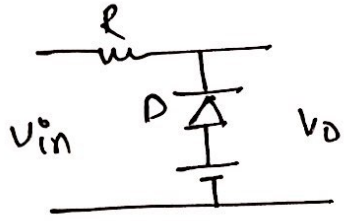
$V_o = V_{in}$ volts

During -ve Half cycle

$V_o = V_d = 0$ (ideal diode).

Qu 3 Draw the output wave form for the following CKT:

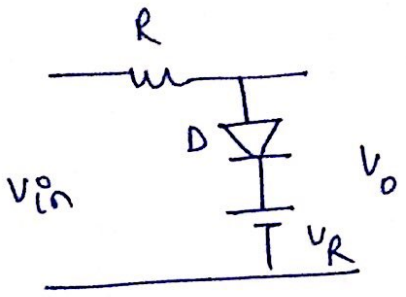
① 

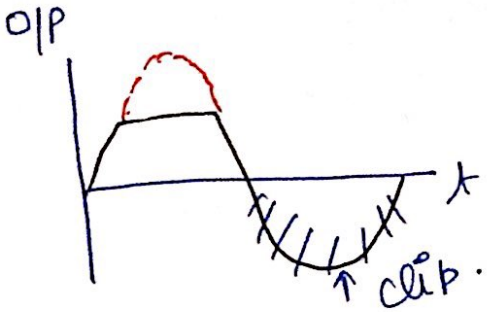
② 

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Sol^n:-

(1)





in +ve Half cycle:

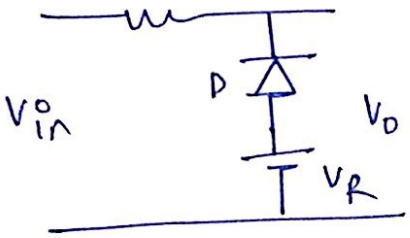
$V_i < V_R$: D = R.B $\Rightarrow V_o = V_{in}$

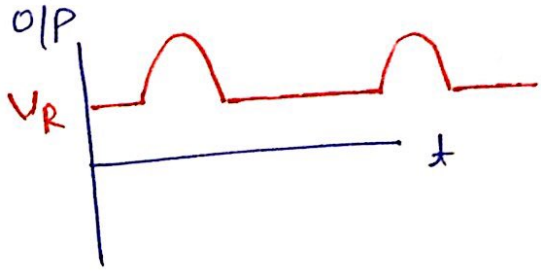
$V_i > V_R$: D = R.B $\Rightarrow V_o = V_R$

in -ve Half cycle:

D = R.B (always) $\Rightarrow V_o = V_{in}$

(2)





During +ve Half cycle:

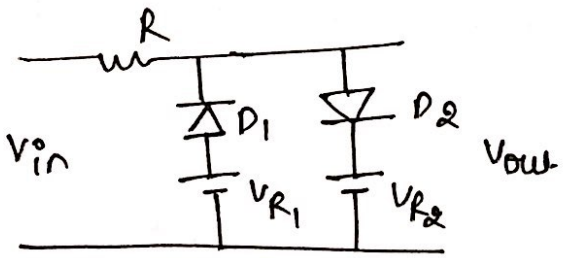
$V_i > V_R \Rightarrow$ D = R.B $\Rightarrow V_o = V_{in}$

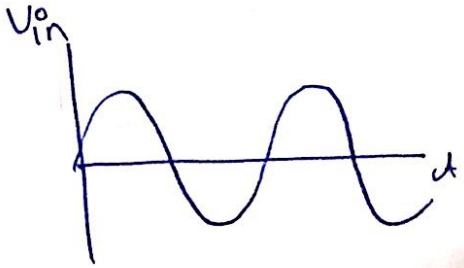
$V_i < V_R \Rightarrow$ D = F.B $\Rightarrow V_o = V_R$

During -ve Half cycle

D = F.B (always) $\Rightarrow V_o = V_R$

Que 4 Draw the output waveform for:





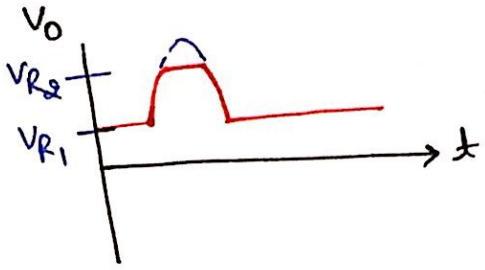
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Soln:- For +ve half cycle:

$V_{in} \leq V_{R_1} \Rightarrow V_o = V_{R_1}$

$V_{in} \geq V_{R_2} \Rightarrow V_o = V_{R_2}$

and $V_{R_1} < V_{in} < V_{R_2} \Rightarrow V_o = V_{in}$

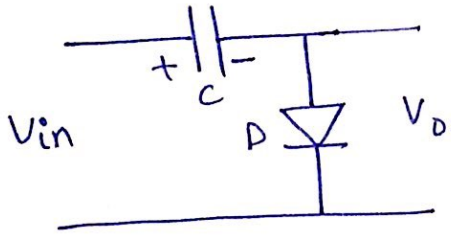


→ **Clamper circuit:**

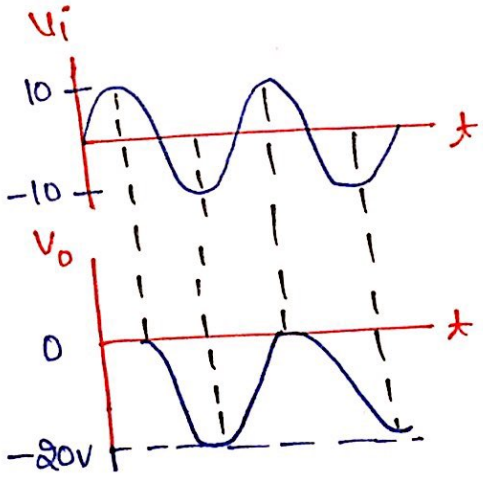
Clamping is a process of introducing a dc level into a signal.

Basic circuit elements: capacitor and diode.

1> **Negative diode clamper:**

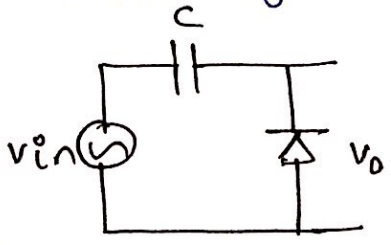


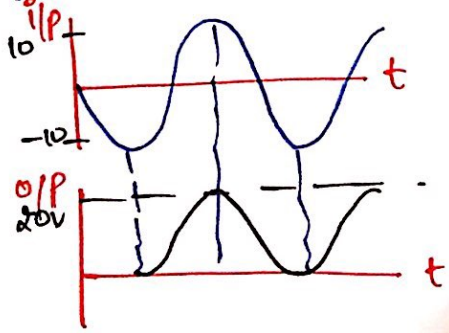
$V_D = V_{in} - V_C$



2> **Positive clamper:**

Introduce +ve dc voltage equal to the peak of input signal.



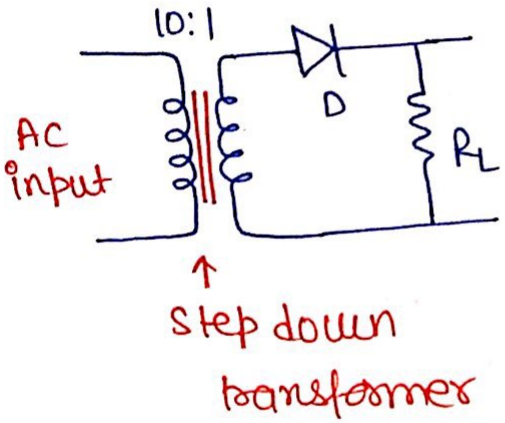


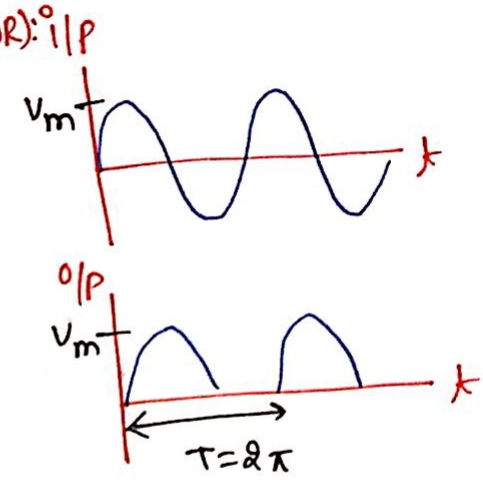
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→ **Rectifiers:**

used to convert ac signal to Pulse like dc.

1) **Half wave Rectifier (HWR):**





average value of Half wave Rectified o/p:

$$V_{avg.} = \frac{1}{2\pi}\int_0^{2\pi} f(\theta)\,d\theta$$

$$= \frac{1}{2\pi}\int_0^{\pi} f(\theta)\,d\theta + \frac{1}{2\pi}\int_{\pi}^{2\pi} f(\theta)\,d\theta \;\to\; 0$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m \sin\theta\,d\theta \Rightarrow \frac{V_m}{\pi}$$

$$\boxed{V_{avg.} = \frac{V_m}{\pi}}$$

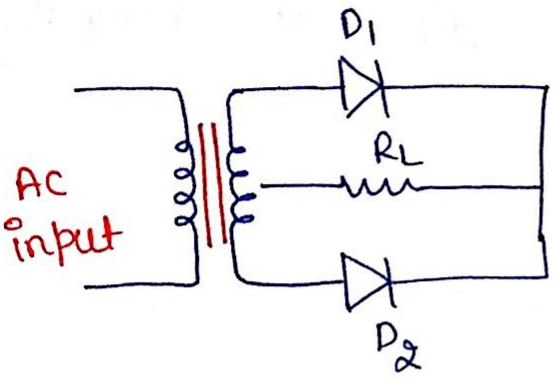
RMS value of Half wave Rectified o/p:

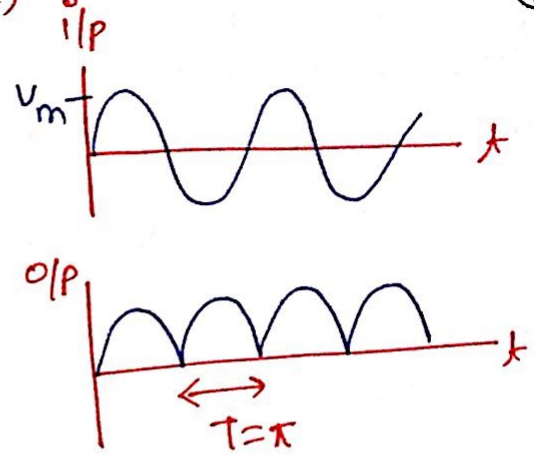
$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} f^2(\theta)\,d\theta} = \frac{V_m}{2}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

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2) Full wave Rectifier: (FWR)





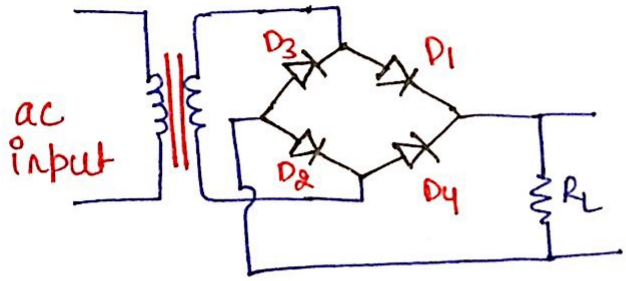
average value of FWR o/p:

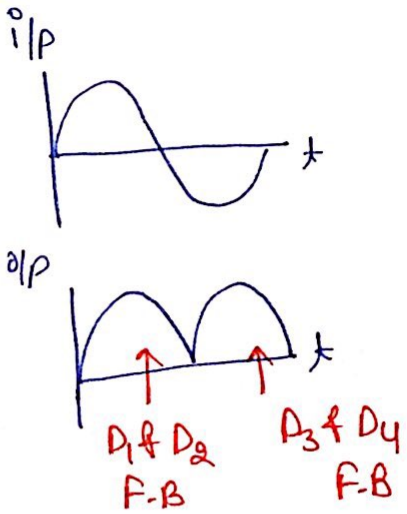
$$V_{avg.} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\theta \, d\theta = \frac{2V_m}{\pi} \Rightarrow 0.637\, V_m$$

RMS value of FWR o/p:

$$V_{rms} = \sqrt{\frac{V_m^2}{\pi}\int_0^{\pi} \sin^2\theta \, d\theta} = \frac{V_m}{\sqrt{2}}$$

Bridge full wave Rectifier:





Ripple factor:

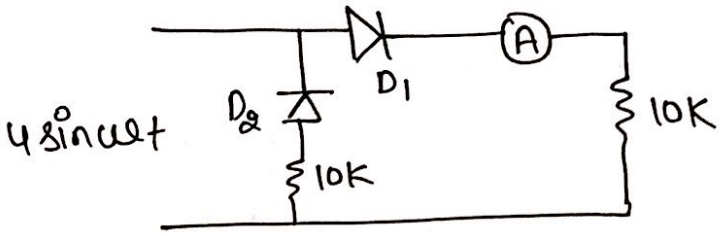
$$\text{Ripple factor} = \sqrt{\left(\frac{V_{rms}}{V_{avg}}\right)^2 - 1}$$

→ Ripple factor for HWR: 1.21

→ Ripple factor for FWR: 0.482

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Que 1 In circuit of given figure that diodes are ideal and ammeter is an average indicating A then ammeter will read:



a) $0.4\sqrt{2}$ mA b) 0.4 mA c) $\frac{0.8}{\pi}$ mA d) $\frac{0.4}{\pi}$ mA

Soln:- take Ⓐ → as reference

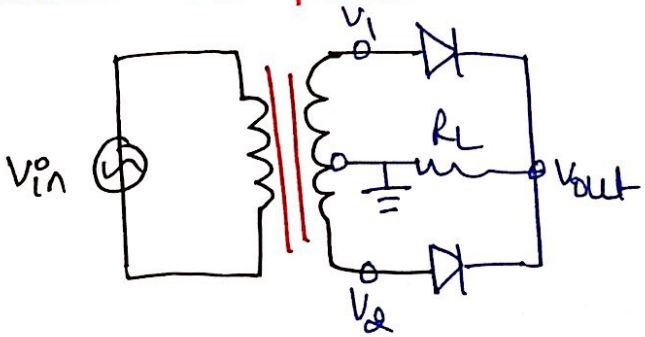
works for +ve half cycle & Doesn't work for -ve Half cycle i.e HWR

$$V_{avg} = \frac{V_m}{\pi} = \frac{4}{\pi}$$

$$I_{avg.} = \frac{V_{avg}}{R} = \frac{4}{\pi \times R} = \frac{0.4}{\pi} \quad (\text{as } R=10)$$

D

Que 2 For the rectifier circuit shown in figure, the sinusoidal voltage (V_1 or V_2) at the output of the transformer has a maximum value of 10V. The load resistance R_L is 1KΩ. If I_{avg} is the average current through the resistor R_L the circuit corresponds to a:



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a) FWR with $I_{avg} = \frac{20}{\pi}$ mA b) HWR with $I_{avg} = \frac{20}{\pi}$ mA

c) HWR with $I_{avg} = \frac{10}{\pi}$ mA d) FWR with $I_{avg} = \frac{10}{\pi}$ mA

Soln:- given configuration is FWR

$$V_{avg} = \frac{V_m}{2\pi} = \frac{2\times 10}{\pi} = \frac{20}{\pi}$$

$$I_{avg} = \frac{V_{avg}}{R} = \frac{20}{\pi \times 1k} = \frac{20}{\pi}\text{ mA}$$

[A]

Que3 If the peak output voltage of a FWR is 10V, its dc voltage is:

a) 10.0V b) 1.07V c) 6.36V d) 3.18V

Soln:- For FWR

$$V_{DC} = \frac{2V_{rms}}{\pi} = \frac{2\times 10}{3.14} = 6.36V$$

[C]

Que4 An ac voltage of 220 V (rms) is applied to the primary of a 10:1 step down transformer. The secondary of the transformer is centre tapped and connected to a FWR rectifier with a load resistance. The DC voltage appearing at the load is:

a) $22/\pi$ b) $31/\pi$ c) $62/\pi$ d) $44/\pi$

Soln:- For FWR: $I_{DC} = \frac{2V_{rms}}{\pi R_L} \Rightarrow V_{DC} = \frac{2V_{rms}}{\pi R_L} \times R_L$

$$V_{DC} = \frac{2V_{rms}}{\pi} = \frac{2}{\pi} \times \frac{220}{10} = \frac{44}{\pi}$$

[D]

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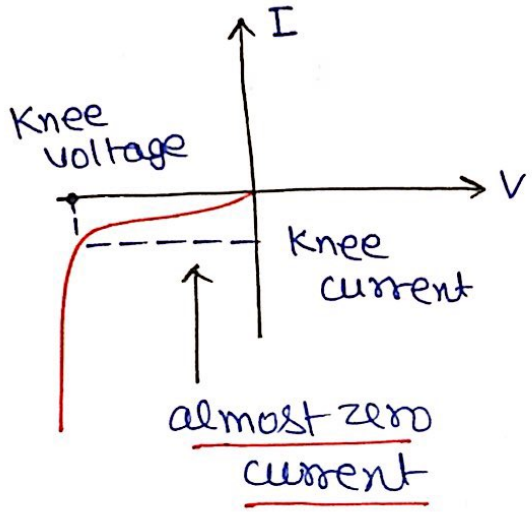
→ **Zener Diode:**

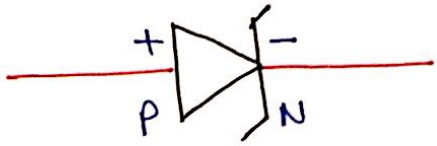
is also known as breakdown (p-n) function diode with high doping [1: 10^5 to 10^3]

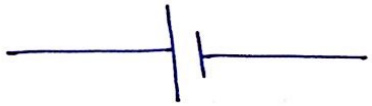
Doping →
- low : $1-10^9$ to 10^{10}
- moderate : $1-10^6$
- High : $1-10^3$ to 10^5

Zener diode is mainly used in: R.B condition.

Zener diode behaves a ordinary diode in: F.B







0.7V under F.B

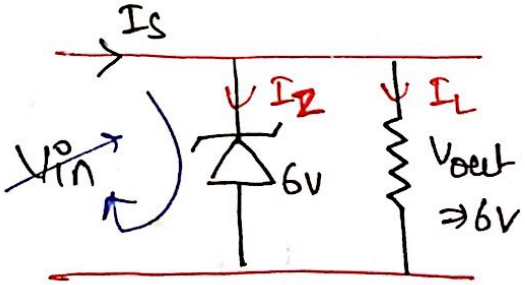
Zener diode as voltage Regulator:

The variation in the output is mainly because of two region:

→ change in supply

→ change in the load.

To maintain constant o/p voltage zener diode is connected in parallel with load.



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$P_{max} = I_Z V_Z$ $\quad$ $P_{min} = I_Z V_{Zmin} \approx 0$

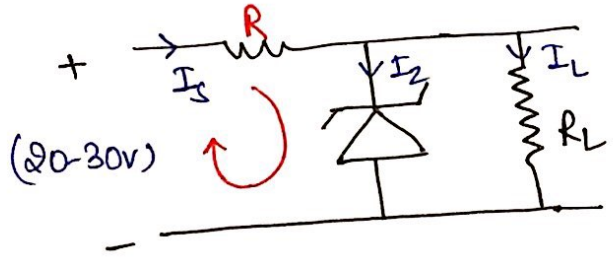
$$I_{max} = \frac{P_{max}}{V_Z}$$

To solve Problems:

(1) apply loop

(2) $I_S = I_Z + I_L$

Que! For the given zener regulator circuit shown determine the range R assume load current $I_L = 10\,mA$, $I_Z = 1mA$



Soln:- $I_S = I_Z + I_L = (1+10) \Rightarrow 11mA$

apply loop

$$-V_{in} + R \times I_S + 10V = 0$$

$$R = \frac{V_{in} - 10}{I_S}$$

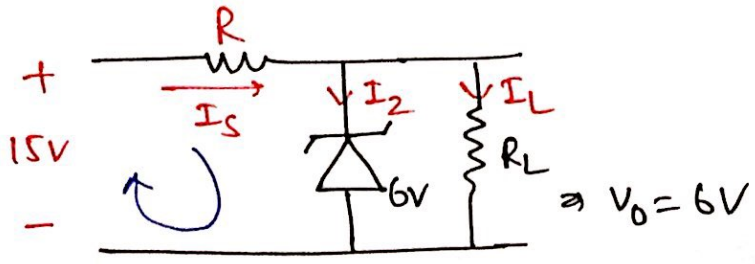
$$R_{min} = \frac{(20-10)}{11\,mA} = 909\Omega$$

$$R_{max} = \left(\frac{30-10}{11}\right) = 1818\Omega$$

Range = 909Ω to 1818Ω

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Que 2 Determine the Range R for the given circuit shown. Assume the breakdown voltage $V_{BR}=6V$. knee current $I_{min}=5mA$. Assume load current varies from 100mA–500mA. So that, it maintain a constant output voltage of 6V.



Solⁿ:- $I_S = I_Z + I_L$

$I_{S\,max} = 5mA + 100mA = 105mA$

$I_{S\,max} = 5mA + 500mA = 505mA$

now, apply loop

$$-15V + I_S R + 6V = 0$$

$$I_S = \frac{9V}{R}$$

$$R_{min} = \frac{9V}{I_{S\,max}} = \frac{9V}{505} = 17.82\,\Omega$$

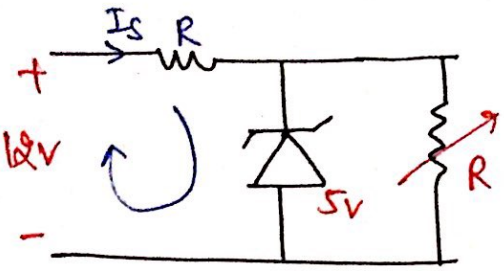
$$R_{max} = \frac{9V}{I_{S\,min}} = \frac{9V}{105} = 85.71\,\Omega$$

Range = 18Ω to 86Ω

Que 3 In the voltage regulator shown in figure, the load current can be vary from (100–500)mA assuming that zener diode is ideal.

a) 7Ω b) 70Ω c) 70/3Ω d) 14Ω

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Soln:- $I_S = I_Z + I_L \approx I_L$ $\quad I_Z = 0$ for ideal zener

now apply loop

$$-12V + 5V + I_S R = 0$$

$$R = 7V / I_S$$

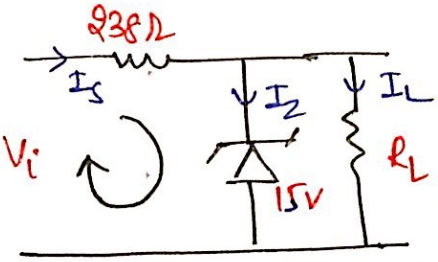
$$R_{max} = \frac{7V}{I_{Smin}} = \frac{7}{100\,mA} = 70\Omega$$

$$R_{min} = \frac{7V}{500}\,mA = 14\Omega$$

$$14\Omega < \frac{70}{3}\Omega < 70\Omega$$

C

Ques 4 find the input voltage of the given circuit



given that the maximum Power drawn is 200mw.

Soln:- $P_{max} = V_Z I_{Zmax} = 200\,mW$

$$I_{Zmax} = \frac{200}{15V} = 13.3\,mA$$

Power through load : $P_L = 150\,mW$

$$V_Z I_L = 150\,mA \Rightarrow I_L = 10\,mA$$

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$I_{S_{max}} = 13.3 + 10 \Rightarrow 23.3\ mA$

$I_{S_{min}} = 0 + 10 \Rightarrow 10\ mA$

now apply loop

$-V_i + 238 \times 10 + 15 = 0$

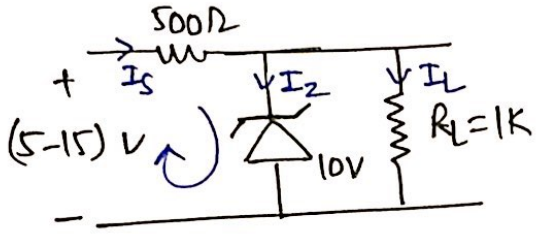
$V_i = 17.38\ V$

$-V_i + 238 \times 23.3 + 15 = 0$

$V_i = 20.545\ V$

$V_i \Rightarrow 17.5$ to $20.5\ V$

Ques: Determine the ratio of maximum to minimum Power at the load for the given circuit diagram



$I_S = I_Z + I_L$

Soln:- For $V_{in} = 15V$

apply loop

$-15V + 500\Omega \times I_S + 10V = 0$

$I_S = \frac{5V}{500} = 10mA$

$P = \frac{V^2}{R} = \frac{100V}{1K}$

$P = 100\ mW$

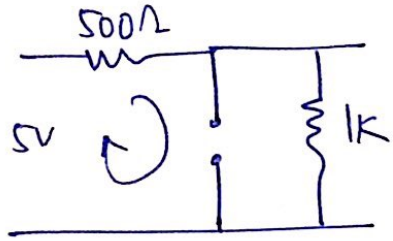
alternate:

$P = I^2R$

$= (10mA)^2 \times 1K$

$P = 100\ mW$

For $V_{in} = 5V$



$-5V + 500I_S + 1K \cdot I = 0$

$I = \frac{5V}{1.5K} = 3.33mA$

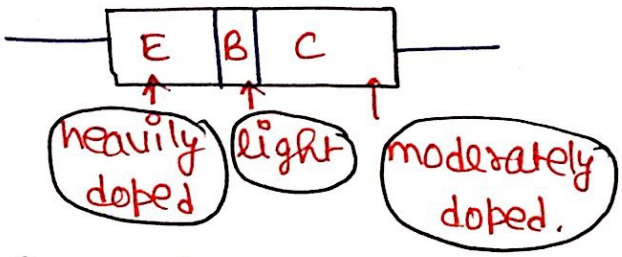
$P = I^2R$

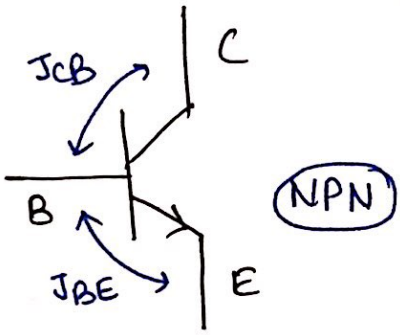
$= (3.33)^2 \times 1K$

$P = 11.09\ mW$

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→ Bipolar Junction Transistor :





emitter: is used to supply the majority carriers.

Base: region through which majority carrier passes & reaches to the collector

collector: majority carriers supplied by emitter are collected at collector.

Region of Transistor:

Region	J_{BE} / J_E	J_{CB} / J_C	Application
active	F.B	R.B	Amplification
Satration	F.B	F.B	Switch ON
cut off	R.B	R.B	Switch OFF

→ By default transistor is in: Active Region.

→ Doping concentration: $D_E > D_C > D_B$

→ width: $W_C > W_E > W_B$

For npn: $I_E = I_C + I_B$

For pnp: $-I_E = I_C + I_B$

→ BJT is a: CCCS

(current controlled current source)

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Configuration in Transistors:

	Common Base	Common emitter	Common collector
input output	emitter collector	Base collector	Base Emitter
current gain	$\alpha = \frac{I_C}{I_E}$ (Low)	$\beta = \frac{I_C}{I_B}$ (med)	$\gamma = \frac{I_E}{I_B}$ (High)
input Resistance	Low	medium	High
output Resistance	High	medium	Low
voltage gain	High	medium	low
Power gain	Low	High	medium
i/p - o/p phase	0	180°	0

Relation between current gain coefficients:

$\alpha = \frac{\beta}{1+\beta}$; $\beta = \frac{\alpha}{1-\alpha}$; $\gamma = 1+\beta$

$\rightarrow$ *** $I_C = \beta I_B + (1+\beta) I_{CBO}$

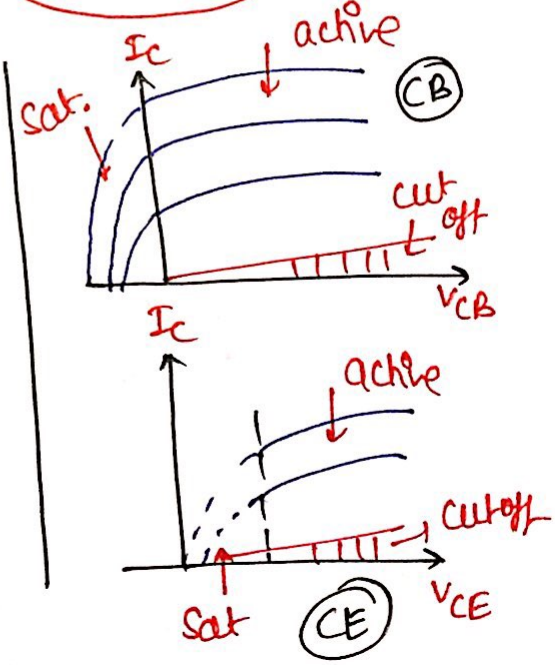
$\rightarrow$ *** $(1+\beta) I_{CBO} = I_{CEO}$

$\rightarrow$ *** $I_C = \alpha I_E + I_{CBO}$

$\rightarrow$ *** $I_E = I_C + I_B$

$\rightarrow$ *** $V_{CE} = V_{BE} + V_{CB}$

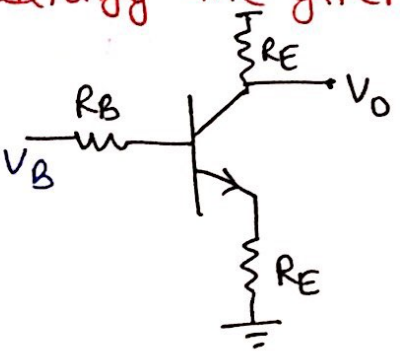
$I_{CEO} > I_{CBO}$



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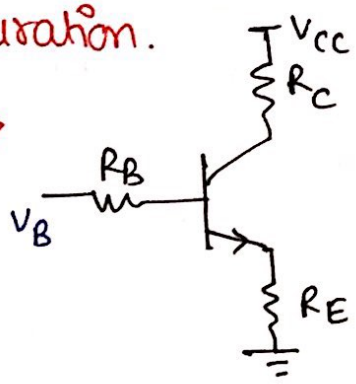
Que:- Identify the given configuration.

a)



Soln:- input ⇒ Base
output ⇒ collector
i.e common Emitter

b)



input = Base
output = Emitter
i.e common collector.

Que:- A transistor is excited by a base current of 10 μA, $\alpha = 0.99$, leakage current 10 μA. Determine all other currents?

Soln:- transistor is excited by Base current
i.e i/p is at Base

CE, OR, CC
↑
most prefer.

$$I_C = \beta I_B + (1+\beta) I_{CEO} \quad -(1)$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

$$I_C = 99 \times 10 + (1+99)10$$

$$= 990\ \mu A + 1000\ \mu A \Rightarrow 1.99\ mA$$

$$I_E = I_C + I_B$$

$$= 1.99\ mA + 0.01\ mA = 2\ mA$$

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Que 3 A transistor is excited by an emitter current of 10mA & $\beta = 99$, leakage current 10 μA. Determine all other current? (OP)

Soln:- $I_E = 10\,mA$, $I_{CBO} = 10\,\mu A$, $\beta = 99$

$$\alpha = \frac{\beta}{1+\beta} = \frac{99}{100}$$

transistor is excited by emitter i.e (CB) OR CC

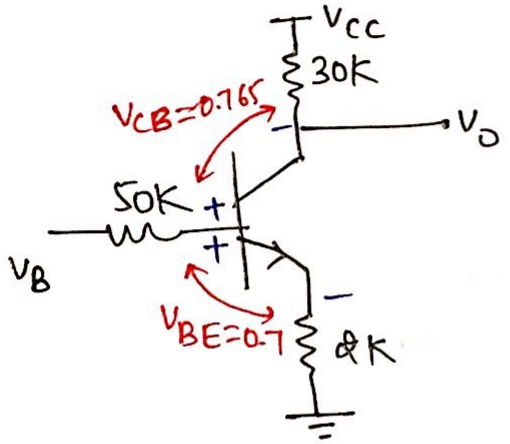
$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = 0.99 \times 10\,mA + 10\,\mu A$$

$$= 9.91\,mA$$

$$I_B = I_E - I_C = 0.09\,mA$$

Que 4 For the given circuit diagram shown, determine the region of operation of transistor? ($\beta = 100$ given)



$V_{CB} \Rightarrow$ R.B

$V_{BE} \Rightarrow$ F.B

i.e active Region.

Approximate analysis of transistor:

$I_C = \beta I_B$ if $\alpha = 1$

$\beta = \infty$

If $I_B = 0 \Rightarrow I_E \simeq I_C$

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Power dissipated in transistor:

$P_{total} = I_C \times V_{CE}$

+ve → consumed

-ve → Delivered.

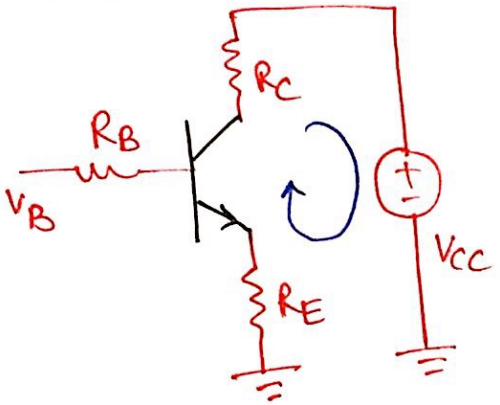
Early Effect:

States the varience inside the transition due to variation in collector base voltage i.e V_{CB}

as V_{CB} ↑es: I_E & I_C ↑es but I_B ↓es

Load line and Q-Point:

a line drawn on the output characteristics



$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

as $\beta \to \infty \Rightarrow I_E = I_E$

$$I_C (R_C + R_E) = V_{CC} - V_{CE}$$

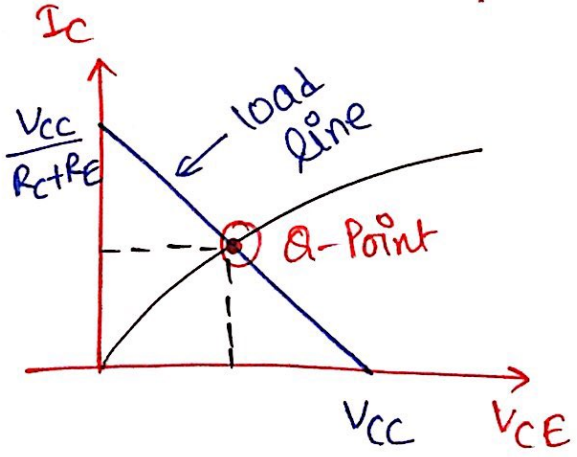
$$\underbrace{I_C}_{y} = \underbrace{\frac{V_{CC}}{R_C+R_E}}_{c} + \underbrace{\left(\frac{-1}{R_C+R_E}\right)}_{m} \underbrace{V_{CE}}_{x}$$

$y = mx + c$

mx

when $V_{CE} = 0$ & $I_C = 0$

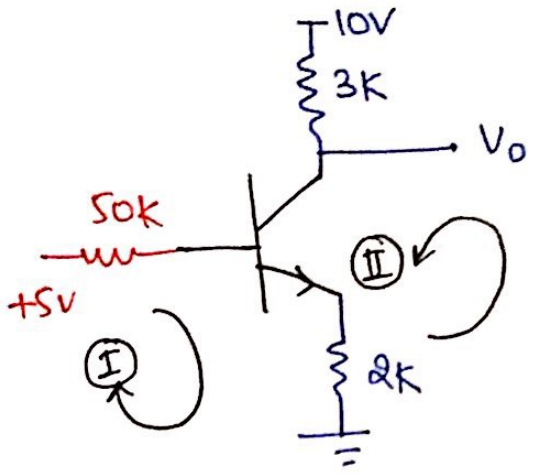
$$I_C = \frac{V_{CC}}{R_C+R_E} \qquad V_{CC} = V_{CE}$$



Q Point (I_C, V_{CE})

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Ques: For the given circuit diagram shown, determine ($\beta = 100$)



a) configuration
b) all currents
c) terminal voltage
d) Power dissipated
e) Region of operation
f) Q.Point & load line.

Sol^{n}:- a) input → Base
output → collector
i.e (CE) Configuration

b) $I_C = \beta I_B = 100 I_B$

apply loop I:

$$-5V + I_B \times 50k + 0.7 + I_E \times 2K = 0$$

$$50 I_B + (I_C + I_B) 2 = 4.3$$

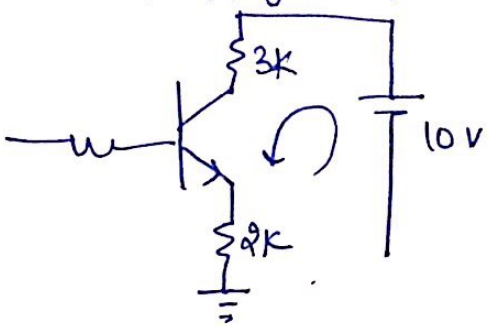
$$52 I_B + 200 I_B = 4.3$$

$$I_B = 0.017\ mA$$

$$I_C = 100 \times 0.017\ mA = 1.7\ mA$$

$$I_E = I_C + I_B = 1.717\ mA$$

c) now, apply loop II:



$$-10V + I_C \times 3K + V_{CE} + I_E \times 2K = 0$$

$$-10V + 5.1V + V_{CE} + 3.417V = 0$$

$$V_{CE} = 1.463V$$

$$V_{CB} = 1.463 - 0.7 = 0.763V$$

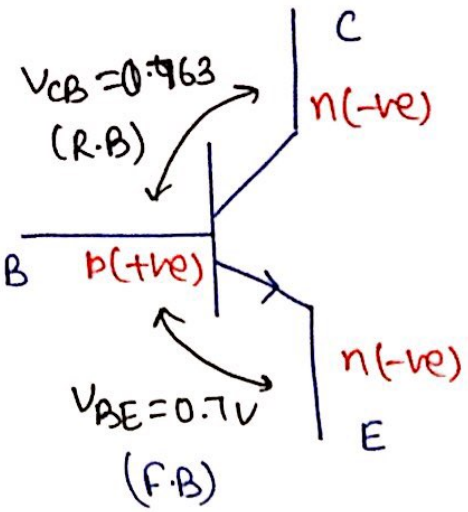
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d) Power dissipated:

$$P_t = I_C \times V_{CE} = 1.7 \times 1.463$$

$$P_t = 2.48\ mW$$

e)

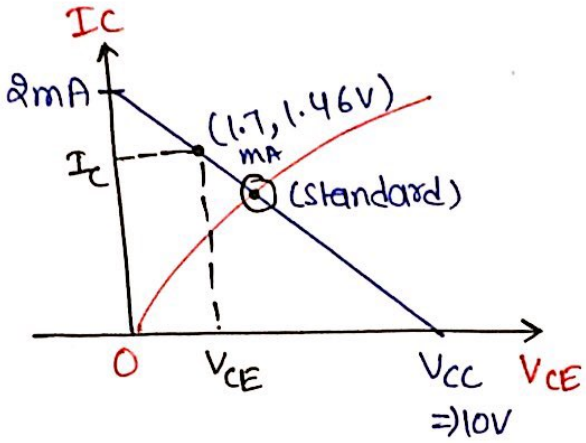


V_{BE} : J_{BE} = F B

J_{CB} = R.B

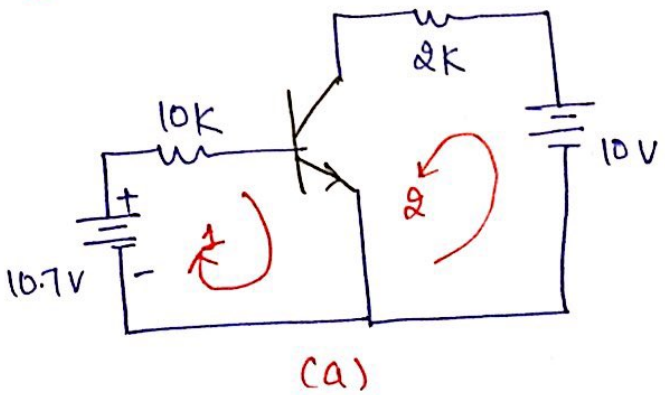
i.e Active Region

f)

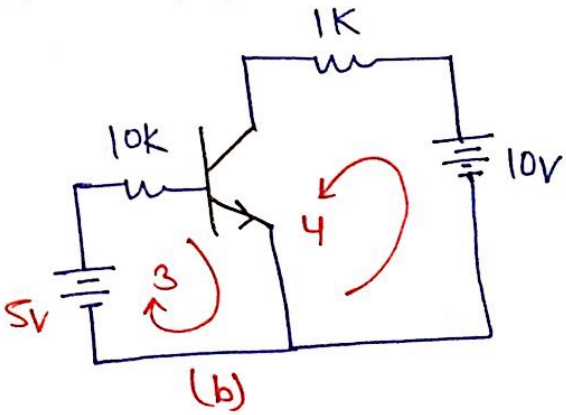


$$\frac{V_{CC}}{R_C + R_E} = \frac{10}{2+3} \Rightarrow 2mA$$

Que 6 Consider the circuits shown in figures (a) and (b)



(a)



(b)

~~Both~~ have current gain (β_{dc}) = 100 & 10 respectively

Find region of operation?

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Soln:- Both have common emitter configuration:

$$I_C = \beta I_B = 100 I_B$$

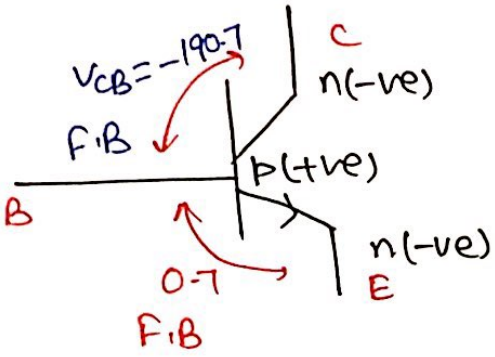
apply loop I:

$$-10.7 + (10K \times I_B) + 0.7 = 0$$

$$I_B = \frac{10}{10K} = 1mA$$

$$I_C = 100 \times 1 = 100mA$$

$$I_E = I_C + I_B = 101mA$$



apply loop II:

$$-10V + 2K I_C + V_{CE} = 0$$

$$V_{CE} = 10 - 200$$

$$V_{CE} = -190V$$

$$V_{CB} = -190 - 0.7$$

$$= -190.7V$$

i.e **Saturation Region**

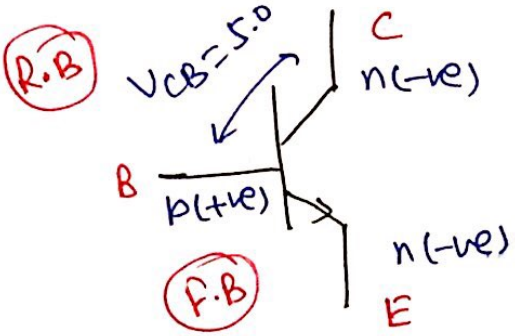
apply loop III:

$$-5V + I_B \times 10 + 0.7 = 0$$

$$I_B = \frac{4.3}{10} = 0.43\,mA$$

$$I_C = 10 \times 0.43 = 4.3\,mA$$

$$I_E = 4.73\,mA$$



apply loop IV:

$$-10V + I_C \times 1K + V_{CE} = 0$$

$$V_{CE} = 10 - 4.3$$

$$V_{CE} = 5.7V$$

$$V_{CB} = 5.7 - 0.7 = 5V$$

i.e **Active Region**

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Stability Factor:

Represents the stability of operating point w.r.t change in any of 3 parameter.

1) Change in temperature:

$$S = \left.\frac{\partial I_C}{\partial I_{CBO}}\right|_{\beta, V_{BE}}$$

2) mismatch in β:

$$S = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CBO}, V_{BE}}$$

3) mismatch in material:

$$S = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CBO}, \beta}$$

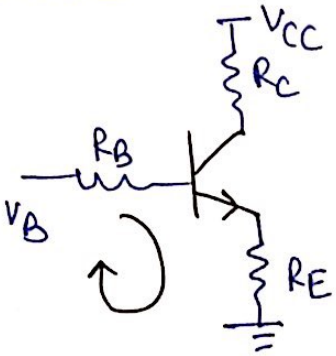
$$\boxed{\frac{\partial I_C}{\partial I_{CBO}} = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}} \quad \text{—①}$$

↑ Stability Factor

→ Stability Factor is as low as Possible

→ Calculate value of $(\partial I_B / \partial I_C)$ for the given Ckt and Put into equation ①

Que: Determine the stability Factor of the given circuit diagram?



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Soln:- apply loop

$$-V_B + I_B R_B + V_{BE} + I_E R_E = 0$$

$$I_B R_B + (I_B + I_C) R_E = V_B - V_{BE}$$

$$I_B (R_B + R_E) = V_B + V_{BE} - I_C R_E$$

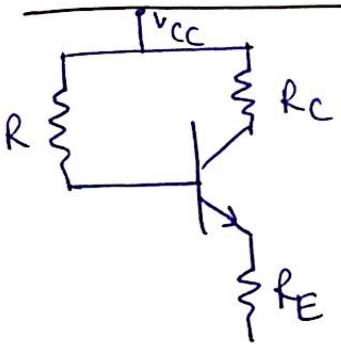
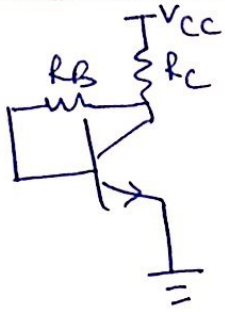
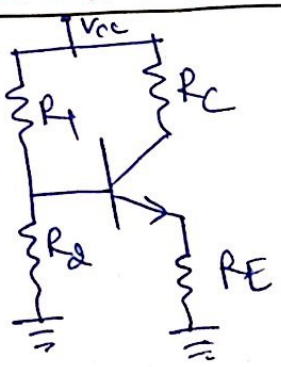
$$I_B = \left(\frac{V_B - V_{BE}}{R_B + R_E}\right) - \frac{I_C R_E}{R_B + R_E}$$

$$\frac{\partial I_B}{\partial I_C} = 0 - \frac{R_E}{R_B + R_E}$$

$$S = \frac{1+\beta}{1+\beta \frac{R_E}{R_E + R_B}}$$

Stablizing circuit:

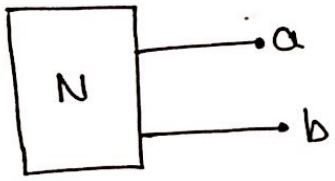
which are used to hold the operating point approximately at one inspective of any change.

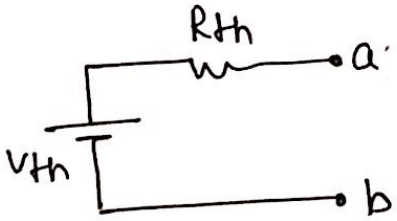
Fixed Biased CKT	collector to Base Biased CKT	self biased / Potential div. / voltage divider
		
$S = 1+\beta$	$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$	$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$
not Practically used	I_C stable	I_C stable

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→ **Thevenin Theorem:** (series CKT)

any network 'N' when seen from two open terminals 'a' & 'b'. It represents a single voltage source 'V_{th}' and a single resistance 'R_{th}' connected in series.





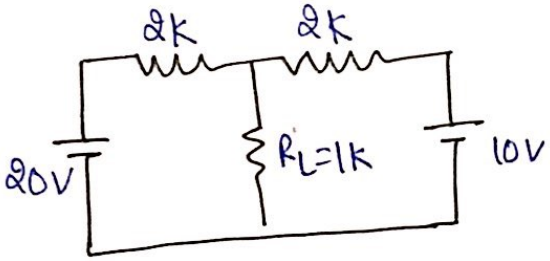
Determination of R_{th}:

1) Short all voltage source
2) open all current source

Determination of V_{th}:

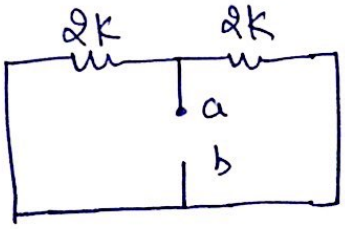
open the two terminals a and b for the determination of V_{th}.

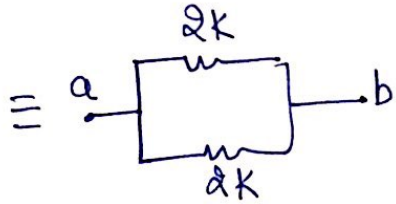
Qu! In the circuit shown in the figure, the thevenin voltage V_{th} and thevenin resistance R_{th} as seen by the load resistance $R_L = 1K$ are respectively.



a) 15V, 1KΩ b) 30V, 4KΩ
c) 20V, 2KΩ d) 10V, 5KΩ

Sol^{n}:- Determination of R_{th}:



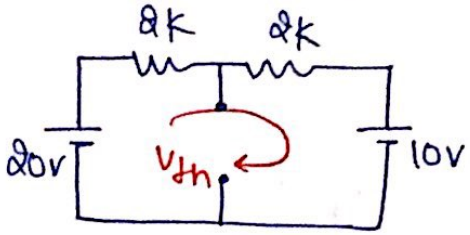


$R_{th} = \frac{1}{2} + \frac{1}{2}$

$R_{th} = 1K$

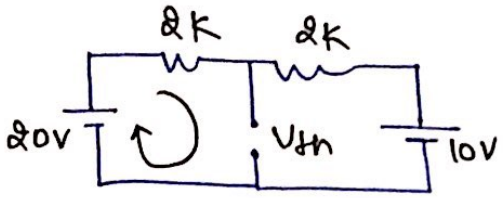
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Determination of V_{th}:



$$-20V + I(2K+2K) + 10V = 0$$

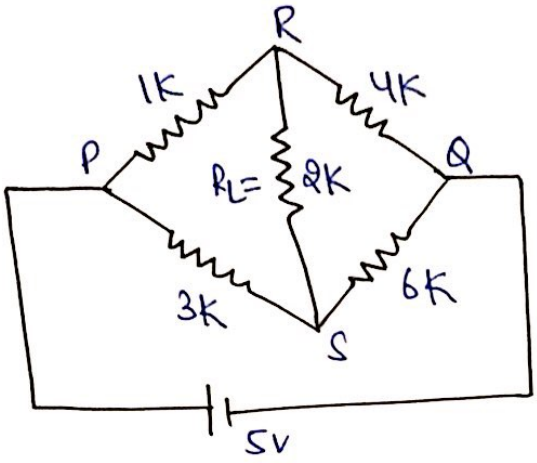
$$I = \frac{10}{4} = 2.5\,mA$$



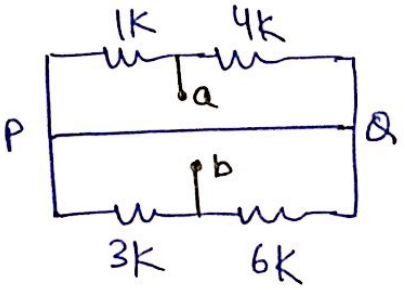
$$-20V + 2.5 \times 2 + V_{th} = 0$$

$$V_{th} = 15V$$

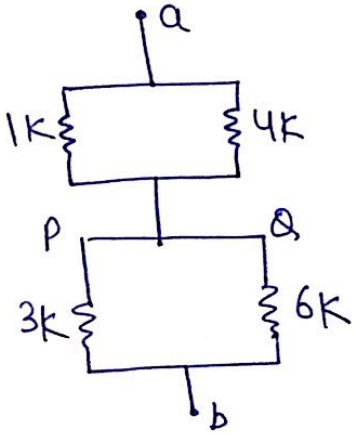
Que: Determine the current across 2kΩ resistance



Soln:- Determination of R_{th}:



≡



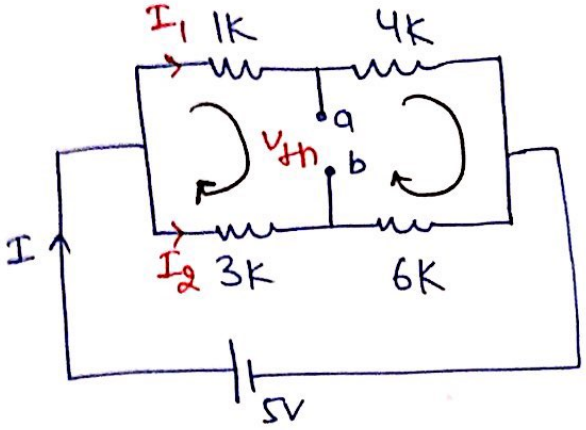
$$\frac{1}{R_{th_1}} = \frac{1}{1} + \frac{1}{4} = \frac{5}{4} \Rightarrow R_{th_1} = \frac{4}{5} = 0.8K$$

$$\frac{1}{R_{th_2}} = \frac{1}{3} + \frac{1}{6} = \frac{9}{18} \Rightarrow R_{th_2} = 2K$$

$$R_{th} = (0.8 + 2) = 2.8K$$

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Determination of V_{th}:



$V = IR$

$I_1 = \frac{5V}{5K} = 1mA$

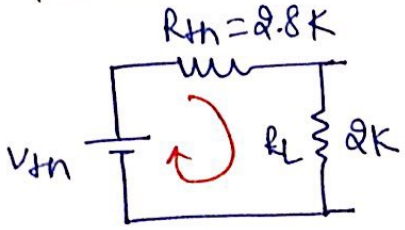
$I_2 = \frac{5V}{9K} = \frac{5}{9}mA$

now, apply loop

$(I_1 \times 1K) + V_{th} - (I_2 \times 3K) = 0$

$V_{th} = \left(\frac{5}{9} \times 3\right) - 1 \times 1 \Rightarrow \frac{5}{3} - 1 \Rightarrow \left(\frac{2}{3}\right)V$

equivalent circuit:

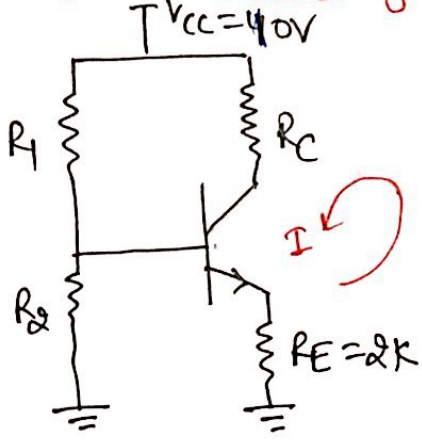


$-\frac{2}{3} + (I \times 2.8) + I \times 2K = 0$

$4.8 \times I = 2/3$

$I = \frac{2}{3} \times \frac{1}{4.8} = \boxed{0.138\,mA}$

Que 3 = Find the value of resistor R_2



$S = 10$

$V_{BE} = 0.7$

β = very large

Q Point = (5V, 1mA)

↑ V_{CE} ↑ $I_C \simeq I_E$

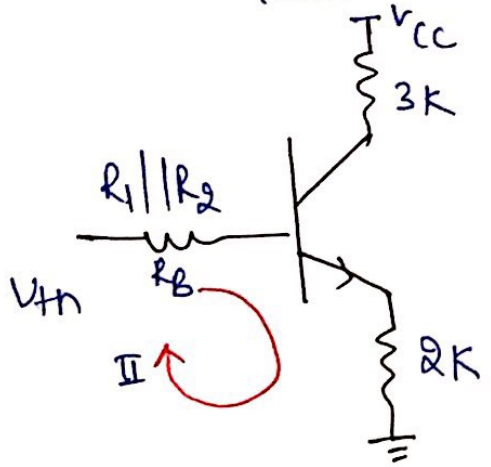
Soln:- apply loop I:

$-10V + I_C R_C + V_{CE} + I_E R_E = 0$

$I_C R_C = 10 - 5 - 2 = 3V$

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$R_C = \frac{3V}{1mA} = 3K$



$R_1||R_2 = \frac{R_1 R_2}{R_1+R_2}$

apply loop II: (0)

$-V_{th} + I_B \times R_B + 0.7 + 2 \times I_E = 0$

$V_{th} = 0.7 + 2.0 = 2.7V$

$S = 10 = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$ $\quad \beta >> 1$

$10 \simeq \frac{1}{\left(\frac{R_E}{R_B+R_E}\right)} = \frac{R_B+R_E}{R_B}$

$R_B = R_{th} = 9R_E$

$R_{th} = 18K$

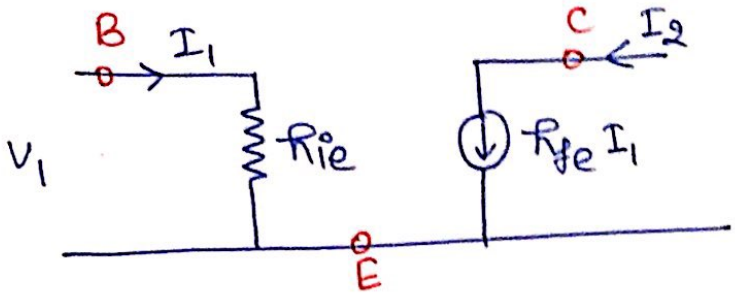
now, $\frac{R_{th}}{V_{th}} = \frac{R_1}{V_{CC}}$

$\frac{18}{2.7} = \frac{R_1}{10} \Rightarrow$ $R_1 = 66K\Omega$

$18 = \frac{R_1 R_2}{R_1+R_2} \Rightarrow$ $R_2 \simeq 25K$

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→ Ac analysis of Transistor (H-Parameter)



(CE) configuration

① $R_{in} = R_{ie}$

② $R_o = \frac{1}{R_{oe}}$

③ $A_{fe} = \frac{I_2}{I_1}$ & $A_{fe} = -\frac{I_L}{I_1}$: current gain

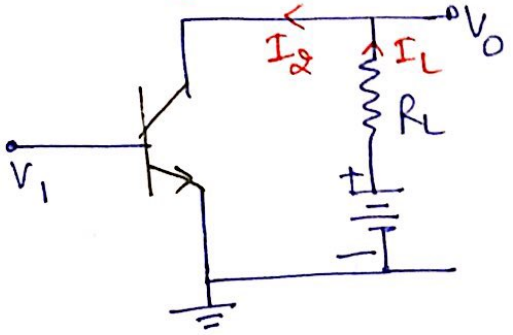
④ Voltage gain: $\frac{V_2}{V_1} = \frac{-A_{fe} \times R_L}{R_{ie}}$

Steps:

1) grounded all DC sources

2) short all capacitors & draw equivalent ckt.

Qu! The transistor in the given circuit has $A_{fe} = 35$ and $R_{ie} = 1000\Omega$. If the load resistance $R_L = 1000\Omega$, the voltage and current gains are, respectively:



a) −35, 35

b) 35, 35

c) 35, 0.97

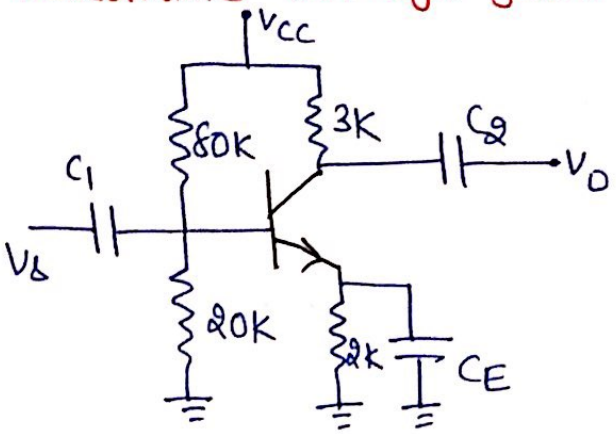
d) 0.98, 35

Sol^{n}- current gain: $A_{fe} = \frac{I_2}{I_1} = 35$

Voltage gain: $\frac{-A_{fe} \times 1000}{R_{ie}} = -35$ (A)

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Que 2 Determine voltage gain and current gain:

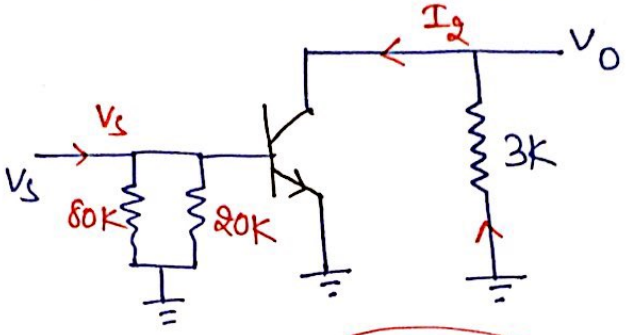


$h_{ie} = 1K$

$h_{fe} = 100$

Soln:- → ground all dc source

→ Replace capacitor by wire.



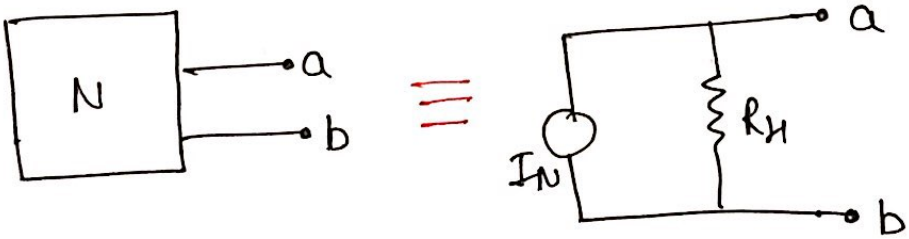
current gain: $h_{fe} = 100$

voltage gain: $\frac{-h_{fe} \times R_L}{h_{ie}} = \frac{-100 \times 3}{1K}$

$= -300$

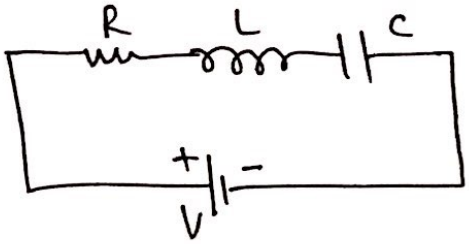
Norton's circuit:

The norton theorem converts an ordinary CKT to an equivalent parallel circuit which is a current source in parallel with a resistor.



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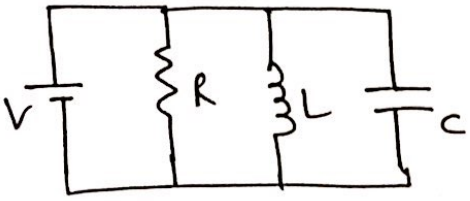
→ Series LCR circuit:



$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

$$V_S^2 = V_R^2 + (V_L - V_C)^2$$

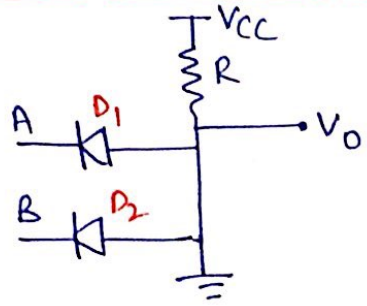
→ Parallel LCR circuit:



$$Z = \frac{1}{\sqrt{\left(\frac{1}{R}\right)^2 + \left(\frac{1}{X_L} - \frac{1}{X_C}\right)^2}}$$

→ Logic gates using Diodes & Transistors:

①

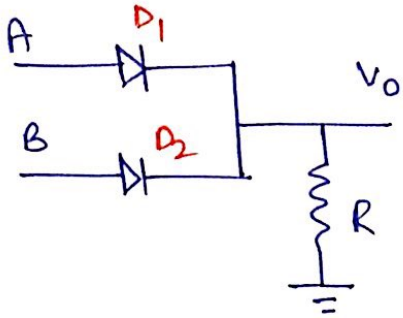


A	B	D_1	D_2	V_o
0	0	F.B	F.B	0
0	1	F.B	R.B	0
1	0	R.B	F.B	0
1	1	R.B	R.B	1

$V_o = A \cdot B$

AND gate

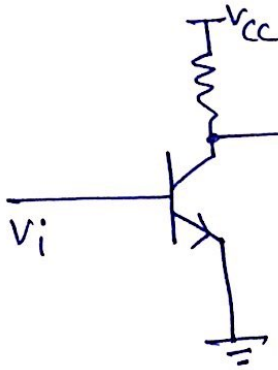
②



$V_o = A + B$

OR gate

③

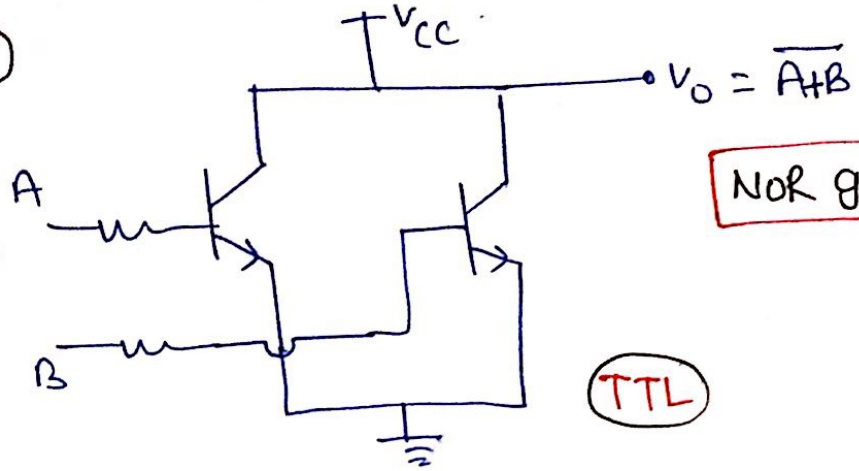


$V_o = \overline{V_i}$

NOT gate

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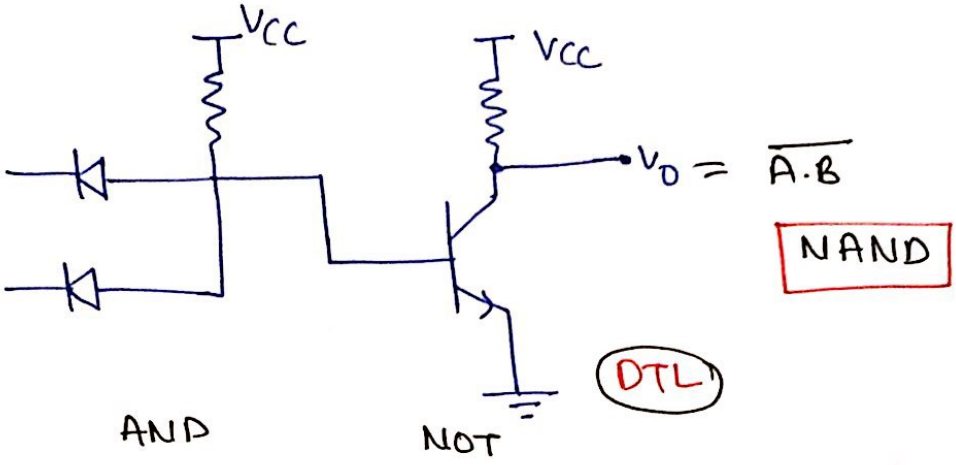
(4)



NOR gate

TTL

(5)



NAND

DTL

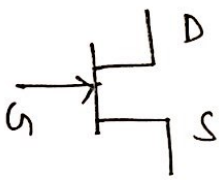
→ Field Effect Transistor: (FET)

1) unipolar Device

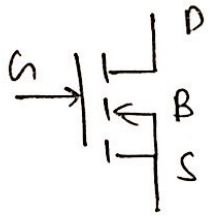
2) thermally stable

3) operation of this device is influenced by $\vec{E}$

VCVS



n-JFET



n-MOSFET

4) FET has more input w.r.t BJT because gate is R.B & $I_G \simeq 0$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$ ***

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when $V_{gs}=0$: $\boxed{I_D = I_{DSS}}$ $I_D \rightarrow$ Drain current

when $V_{gs}=V_p$: $\boxed{I_D=0}$

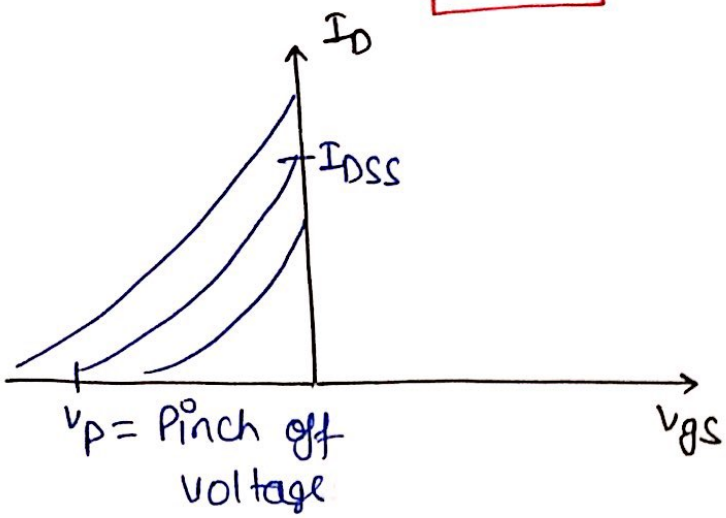


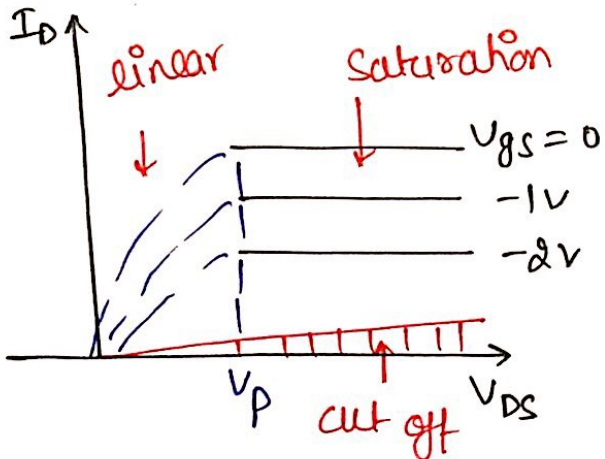
Fig: Transfer characteristics

Transconductance:

$$G_m = \frac{\partial I_D}{\partial V_{GS}} \Rightarrow -\frac{2I_{DSS}}{V_p}\left[1-\frac{V_{gs}}{V_p}\right]$$

$$G_{max} = -\frac{2I_{DSS}}{V_p}$$

output characteristics:



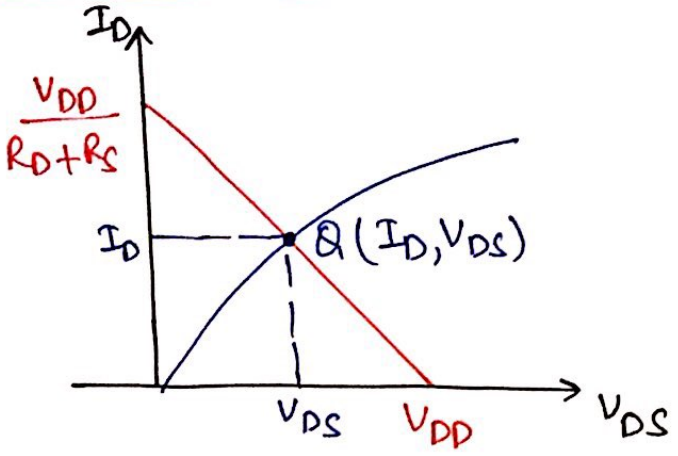
The value of V_{DS} after which I_D becomes constant is called the Pinch off voltage

Power Dissipation:

$$\boxed{P_t = I_D \times V_{DS}}$$

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Load line and Q-Point:



Que 1 An n-channel JFET has 5mA source to drain current at shorted gate (I_{DSS}) and 5V pinch off voltage (V_P). calculate the drain current, for voltage (V_{gs}) of -2.5V?

Soln:-

$$I_D = I_{DSS}\left[1 - \frac{V_{gs}}{V_P}\right]^2$$

$$= I_{DSS}\left[1 - \frac{-2.5}{-5}\right]^2$$

$$= 5mA \times \left[1 - \frac{1}{2}\right]^2 = \boxed{1.25\,mA}$$

Que 2 For an n-channel JFET if V_{gs} changes from -2 to -4V then I_D also changes from 3 to 1 mA. Determine transconductance?

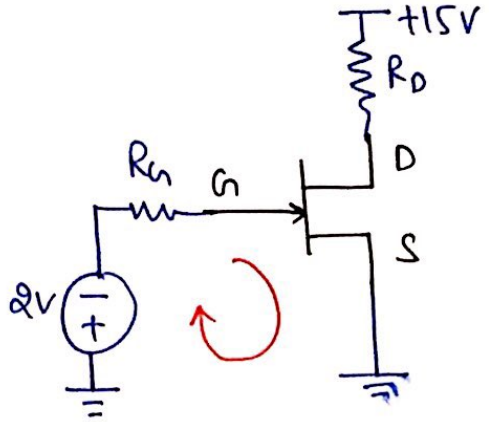
Soln:-

$$G_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{I_{D\,final} - I_{D\,initial}}{V_{gs\,final} - V_{gs\,initial}}$$

$$= \frac{1mA - 3mA}{-4+2} = \boxed{1mA/V}$$

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Que 3 For the given circuit diagram shown determine I_D, g_m and g_{max}. If $I_{DSS} = 10mA$, $V_p = -5V$



$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Soln:- apply loop: $2V + 0 \times R_G + V_{GS} = 0$

$$V_{GS} = -2V$$

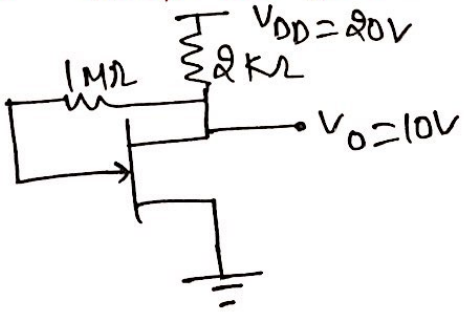
$$I_D = 10mA\left[1 - \frac{-2V}{-5V}\right]^2 = \boxed{3.6mA}$$

$$g_m = \frac{-2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \Rightarrow \frac{-2 \times 10mA}{-5}\left[1 - \frac{2}{5}\right]$$

$$= \boxed{2.4\ mA/V}$$

$$g_{max} = \frac{-2I_{DSS}}{V_P} = \boxed{4mA/V}$$

Que 4 For the given circuit diagram, Determine I_{DSS}, ~~g_m and g_{max}~~ for given CKT. ($V_{GS} = -2V$, $V_P = -10V$)



$$I_D = \frac{(20-10)V}{2K}$$

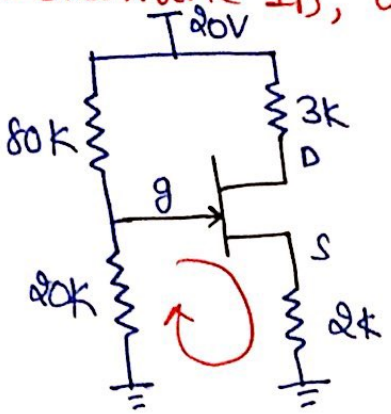
$$I_D = 5mA.$$

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$$5mA = I_{DSS}\left[1-\frac{2}{10}\right]^2 \Rightarrow I_{DSS} \times \frac{16}{25}$$

$$I_{DSS} = \frac{5 \times 25}{16} = \boxed{7.81\ mA}$$

Ques Determine I_D, assume $V_{gs} = -2V$



Soln:- $R_{th} = \frac{20 \times 80}{20+80} = 16k$; $V_{th} = \frac{20 \times 20}{80+20} = 4V$

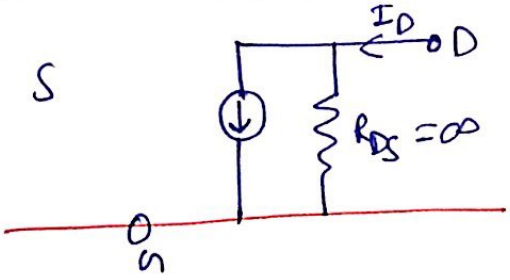
apply loop:

$$-4V + 0 \times 16 - 2V + I_S \times 2k = 0$$

$$I_S = 3mA$$

$$\boxed{I_S = I_D = mA} \quad \& \quad I_g = 0$$

equivalent model of JFET:

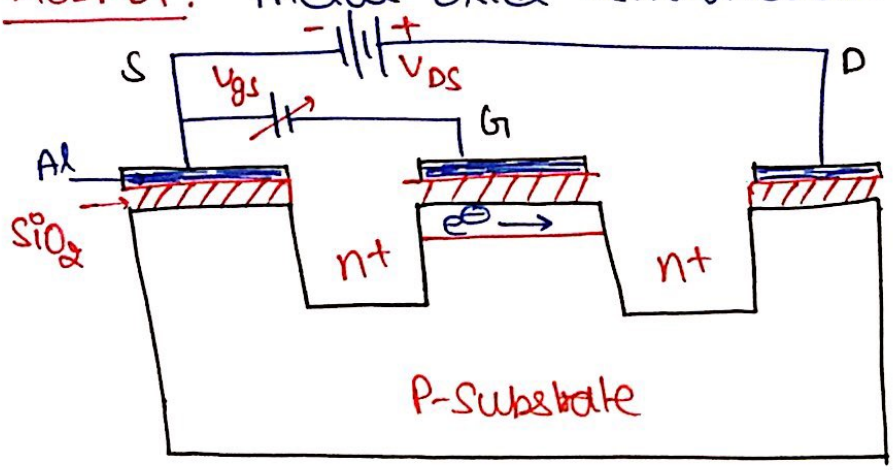


$$g_m = \frac{I_D}{V_{gs}}$$

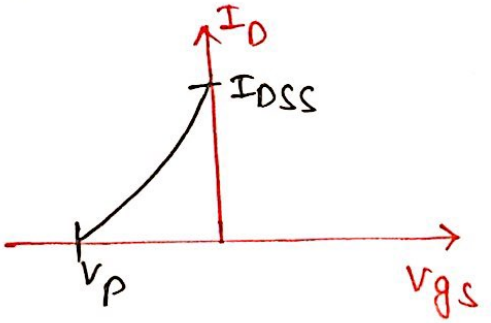
$$\boxed{I_D = V_{gs} \times g_m}$$

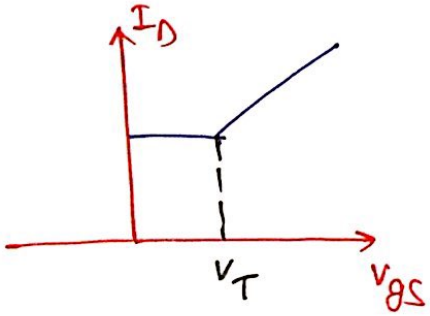
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→ MOSFET: metal oxide semiconductor FET



Depletion n-channel	Enhance n-Channel
used to ↓es the no. of charge carriers in the channel.	used to ↑es the no. of charge carriers in the channel.





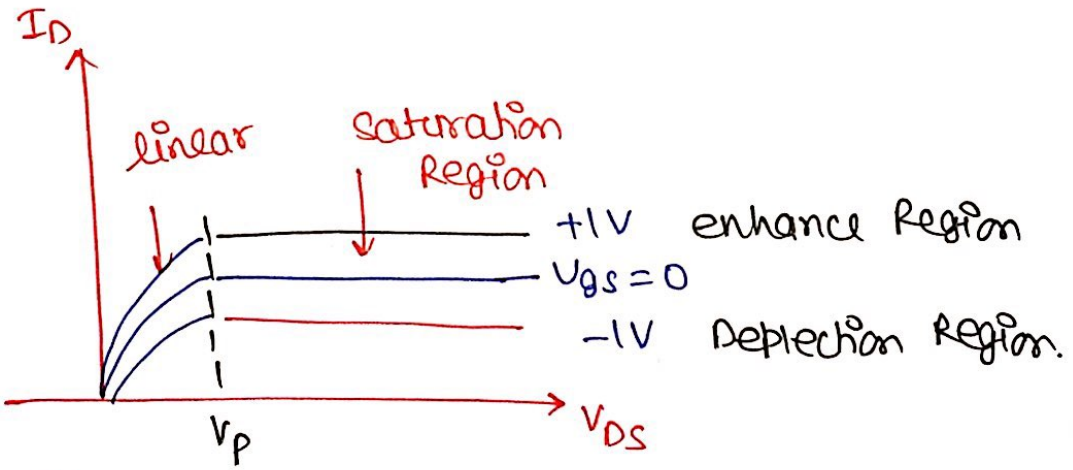
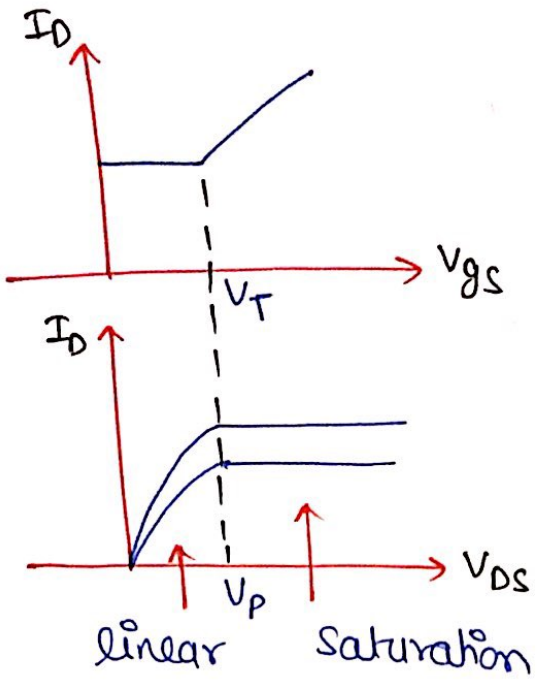


Fig: output characteristics

Oxide capacitance:

*** $C_{ox} = \frac{3.45 \times 10^{-11}}{\text{thickness}}$ F/m²

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$V_p = (V_{DS})_{sat}$

$= V_{gs} - V_T$

Ohmic / linear / triode	Saturation / Pentode Region
$(V_{DS})_{sat} < V_{gs} - V_T$	$(V_{DS})_{sat} > V_{gs} - V_T$
$I_D = \mu_N C_{ox} \left(\frac{W}{L}\right) [V_{gs} - V_T] V_{DS}$ $I_D = k[V_{gs} - V_T] V_{DS}$	$I_D = \frac{1}{2} k [V_{gs} - V_T]^2$
$g = \frac{\partial I_D}{\partial V_{gs}} = k V_{DS}$	$g = k [V_{gs} - V_T]$

Que: Consider n-channel MOSFET with the following Parameters:

current drive strength: $K = 60\,\mu A/V^2$

$(W/L) = 5$

$V_{DS} = 10V$

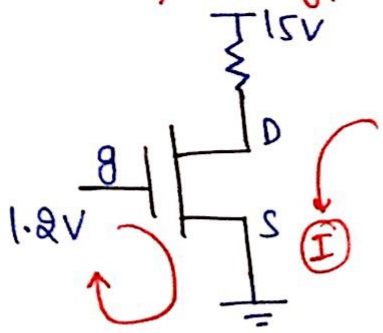
$V_{th} = 0.5V$

Determine the MOSFET's operating point:

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a) ohmic b) cut off c) saturation d) Breakdown

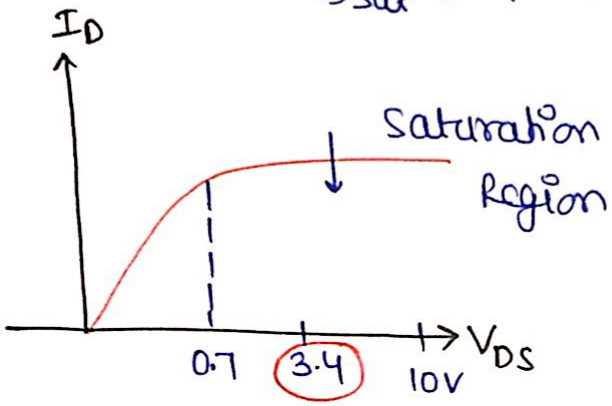
Soln:-



$$(V_{DS})_{sat} = V_{gs} - V_{th}$$
$$= V_{gs} - 0.5$$

apply loop: $-1.2V + V_{gs} = 0 \Rightarrow \boxed{V_{gs} = 1.2V}$

$$(V_{DS})_{sat} = 1.2 - 0.5 = 0.7V$$



$$I_D = K\left(\frac{W}{L}\right)[V_{gs} - V_t]^2$$
$$= 60 \times 5 \times (0.7)^2 = 147\ \mu A$$

apply loop I:

$$-15V + (80 \times 147\ \mu A) + V_{DS} = 0$$
$$V_{DS} = 15V - 11.76$$
$$= 3.24V$$

C

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